SERIES
690XXA/691XXA
SYNTHESIZED CW/SWEEP GENERATORS

MAINTENANCE MANUAL

Anritsu

490 JARVIS DRIVE
MORGAN HILL, CA 95037-2809

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DECLARATION OF CONFORMITY

Manufacturer's Name: ANRITSU COMPANY

Manufacturer's Address: Microwave Measurements Division
490 Jarvis Drive
Morgan Hill, CA 95037-2809
USA

declares that the product specified below:

Product Name: Synthesized CW / Sweep / Signal Generator

Model Number: 690XXA, 691XXA, 692XXA, 693XXA

conforms to the requirement of:

EMC Directive 89/336/EEC as amended by Council Directive 92/31/EEC & 93/68/EEC
Low Voltage Directive 73/23/EEC as amended by Council directive 93/68/EEC

Electromagnetic Interference:

Emissions: CISPR 11:1990/EN55011:1991 Group 1 Class A

Immunity:
IEC 1000-4-2:1995/prEN50082-1:1995 - 4kV CD, 8kV AD
IEC 1000-4-3:1993/ENV50140:1994 - 3V/m
IEC 1000-4-4:1995/prEN50082-1:1995 - 0.5kV SL, 1kV PL
IEC 1000-4-5:1995/prEN50082-1:1995 - 0.5kV - 1kV LN
0.5kV - 1kV NG
0.5kV - 1kV GL

Electrical Safety Requirement:

Product Safety: IEC 1010-1:1990 + A1/EN61010-1:1993

Jean Blais
Manager of Corporate Quality

Morgan Hill, CA

5-SEPT-97
Date

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Chapter 1
General Information

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Figure 1-1. *Typical Series 690XXA/691XXA Synthesized CW/Sweep Generator (Model 69169A Shown)*

Chapter 1
General Information

1-1 SCOPE OF MANUAL

This manual provides service information for all models of the Series 690XXA Synthesized CW Generator and the Series 691XXA Synthesized Sweep Generator. The service information includes replaceable parts information, functional circuit descriptions, block diagrams, performance verification tests, and procedures for calibration, troubleshooting, and assembly/subassembly removal and replacement. (Throughout this manual, the term *690XXA/691XXA* is used to refer to the instrument.) Manual organization is shown in the table of contents.

NOTE

Service information for the series 690XXA CW generators and series 691XXA sweep generators is combined into one manual because identical model numbers of each series contain the same assemblies, subassemblies, and components. Differences between the series are noted where applicable throughout the manual.

1-2 INTRODUCTION

This chapter provides a general description of the Series 690XXA/691XXA Synthesized CW/Sweep Generators, identification numbers, related manuals, and options. Information is included concerning level of maintenance, replaceable subassemblies and RF components, exchange assembly program, and preventive maintenance. Static-sensitive component handling precautions and lists of exchangeable subassemblies and recommended test equipment are also provided.

1-3 DESCRIPTION

The Series 690XXA Synthesized CW Generator and the Series 691XXA Synthesized Sweep Generator are microprocessor-based, synthesized signal sources with high resolution phase-lock capability. They generate both discrete CW frequencies and broad (full range) and narrow band sweeps across the frequency range of 10 MHz to 65 GHz. All functions of the 690XXA/691XXA are fully controllable locally from the front panel or remotely (except for power on/standby) via the IEEE-488 General Purpose Interface Bus (GPIB).

The Series 690XXA Synthesized CW Generator and the Series 691XXA Synthesized Sweep Generator each presently consists of 15 models covering a variety of frequency ranges and power levels. Table 1-1, on pages 1-4 and 1-5, lists models, frequency ranges, and maximum leveled output.

Table 1-1. *Series 690XXA/691XXA Models (1 of 2)*

69XXXA Model	Frequency (GHz)	Output Power	Output Power w/Step Attenuator
69X37A	2.0 – 20.0 GHz	+13.0 dBm	+11.0 dBm
69X45A	0.5 – 20.0 GHz	+13.0 dBm	+11.0 dBm
69X47A	0.01 – 20.0 GHz	+13.0 dBm	+11.0 dBm
69X53A	2.0 – 20.0 GHz 20.0 – 26.5 GHz	+9.0 dBm +6.0 dBm	+7.0 dBm +3.5 dBm
69X55A	0.5 – 2.2 GHz 2.2 – 20.0 GHz 20.0 – 26.5 GHz	+13.0 dBm +9.0 dBm +6.0 dBm	+11.0 dBm +7.0 dBm +3.5 dBm
69X59A	0.01 – 2.0 GHz 2.0 – 20.0 GHz 20.0 – 26.5 GHz	+13.0 dBm +9.0 dBm +6.0 dBm	+11.0 dBm +7.0 dBm +3.5 dBm
69X63A	2.0 – 20.0 GHz 20.0 – 40.0 GHz	+9.0 dBm +6.0 dBm	+7.0 dBm +3.0 dBm
69X65A	0.5 – 2.2 GHz 2.2 – 20.0 GHz 20.0 – 40.0 GHz	+13.0 dBm +9.0 dBm +6.0 dBm	+11.0 dBm +7.0 dBm +3.0 dBm
69X69A	0.01 – 2.0 GHz 2.0 – 20.0 GHz 20.0 – 40.0 GHz	+13.0 dBm +9.0 dBm +6.0 dBm	+11.0 dBm +7.0 dBm +3.0 dBm
69X75A	0.5 – 2.2 GHz 2.2 – 20.0 GHz 20.0 – 40.0 GHz 40.0 – 50.0 GHz	+11.0 dBm +10.0 dBm +2.5 dBm +2.5 dBm	+10.0 dBm +8.5 dBm 0.0 dBm –1.0 dBm
69X77A	0.01 – 2.0 GHz 2.0 – 20.0 GHz 20.0 – 40.0 GHz 40.0 – 50.0 GHz	+12.0 dBm +10.0 dBm +2.5 dBm +2.5 dBm	+10.0 dBm +8.5 dBm 0.0 dBm –1.0 dBm
69X85A	0.5 – 2.2 GHz 2.2 – 20.0 GHz 20.0 – 40.0 GHz 40.0 – 50.0 GHz 50.0 – 60.0 GHz	+11.0 dBm +10.0 dBm +2.5 dBm +2.0 dBm +2.0 dBm	+10.0 dBm +8.5 dBm 0.0 dBm –1.5 dBm –2.0 dBm
69X87A	0.01 – 2.0 GHz 2.0 – 20.0 GHz 20.0 – 40.0 GHz 40.0 – 50.0 GHz 50.0 – 60.0 GHz	+12.0 dBm +10.0 dBm +2.5 dBm +2.0 dBm +2.0 dBm	+10.0 dBm +8.5 dBm 0.0 dBm –1.5 dBm –2.0 dBm
69X95A	0.5 – 2.2 GHz 2.2 – 20.0 GHz 20.0 – 40.0 GHz 40.0 – 50.0 GHz 50.0 – 65.0 GHz	+11.0 dBm +10.0 dBm +2.5 dBm 0.0 dBm –2.0 dBm	Not Available

Table 1-1. *Series 690XXA/691XXA Models (2 of 2)*

69XXXA Model	Frequency (GHz)	Output Power	Output Power w/Step Attenuator
69X97A	0.01 – 2.0 GHz 2.0 – 20.0 GHz 20.0 – 40.0 GHz 40.0 – 50.0 GHz 50.0 – 65.0 GHz	+12.0 dBm +10.0 dBm +2.5 dBm 0.0 dBm –2.0 dBm	Not Available
With Option 15A (High Power) Installed			
69X37A	2.0 – 20.0 GHz	+17.0 dBm	+15.0 dBm
69X45A	0.5 – 2.2 GHz 2.2 – 20.0 GHz	+13.0 dBm +17.0 dBm	+11.0 dBm +15.0 dBm
69X47A	0.01 – 2.0 GHz 2.0 – 20.0 GHz	+13.0 dBm +17.0 dBm	+11.0 dBm +15.0 dBm
69X53A	2.0 – 20.0 GHz 20.0 – 26.5 GHz	+13.0 dBm +10.0 dBm	+11.0 dBm +7.5 dBm
69X55A	0.5 – 2.2 GHz 2.2 – 20.0 GHz 20.0 – 26.5 GHz	+13.0 dBm +13.0 dBm +10.0 dBm	+11.0 dBm +11.0 dBm +7.5 dBm
69X59A	0.01 – 2.0 GHz 2.0 – 20.0 GHz 20.0 – 26.5 GHz	+13.0 dBm +13.0 dBm +10.0 dBm	+11.0 dBm +11.0 dBm +7.5 dBm
69X63A	2.0 – 20.0 GHz 20.0 – 40.0 GHz	+13.0 dBm +6.0 dBm	+11.0 dBm +3.0 dBm
69X65A	0.5 – 2.2 GHz 2.2 – 20.0 GHz 20.0 – 40.0 GHz	+13.0 dBm +13.0 dBm +6.0 dBm	+11.0 dBm +11.0 dBm +3.0 dBm
69X69A	0.01 – 2.0 GHz 2.0 – 20.0 GHz 20.0 – 40.0 GHz	+13.0 dBm +13.0 dBm +6.0 dBm	+11.0 dBm +11.0 dBm +3.0 dBm
69X75A	0.5 – 50.0 GHz	Standard	Standard
69X77A	0.01 – 50.0 GHz	Standard	Standard
69X85A	0.5 – 60.0 GHz	Standard	Standard
69X87A	0.01 – 60.0 GHz	Standard	Standard
69X95A	0.5 – 65.0 GHz	Standard	Not Available
69X97A	0.01 – 65.0 GHz	Standard	Not Available

1-4 IDENTIFICATION NUMBER

All ANRITSU instruments are assigned a unique six-digit ID number, such as “603005”. The ID number is imprinted on a decal that is affixed to the rear panel of the unit. Special-order instrument configurations also have an additional *special* serial number tag attached to the rear panel of the unit.

When ordering parts or corresponding with ANRITSU Customer Service, please use the correct serial number with reference to the specific instrument's model number (i.e., Model 69147A Synthesized Sweep Generator, Serial No. 603005).

1-5 ELECTRONIC MANUAL

This manual is available on CD ROM as an Adobe Acrobat Portable Document Format (∗.pdf) file. The file can be viewed using Acrobat Reader, a free program that is also included on the CD ROM. The file is "linked” such that the viewer can choose a topic to view from the displayed "bookmark” list and "jump” to the manual page on which the topic resides. The text can also be word-searched. Contact ANRITSU Customer Service for price and availablility.

1-6 RELATED MANUALS

This is one of a four manual set that consists of an Operation Manual, a GPIB Programming Manual, a SCPI Programming Manual, and a Maintenance Manual.

Operation Manual This manual provides instructions for operation of the 690XXA/691XXA using the front panel controls. It also includes general information, performance specifications, installation instructions, and operation verification procedures. The ANRITSU part number for the Series 690XXA Operation Manual is 10370-10300; the part number for the Series 691XXA Operation Manual is 10370-10306.

GPIB Programming Manual This manual provides information for remote operation of the 690XXA/691XXA using Product Specific commands sent from an external controller via the IEEE 488 General Purpose Interface Bus (GPIB). It contains a complete listing and description of all 690XXA/691XXA GPIB Product Specific commands and several programming examples. The ANRITSU part number for the Series 690XXA GPIB Programming Manual is 10370-10302; the part number for the Series 691XXA GPIB Programming Manual is 10370-10308.

SCPI Programming Manual This manual provides information for remote operation of the 690XXA/691XXA using Standard Commands for Programmable Instruments (SCPI) commands sent from an external controller via the

IEEE 488 General Purpose Interface Bus (GPIB). It contains a complete listing and description of each command in the 690XXA/691XXA SCPI command set and examples of command usage. The ANRITSU part number for the Series 690XXA SCPI Programming Manual is 10370-10304; the part number for the Series 691XXA SCPI Programming Manual is 10370-10310.

1-7 OPTIONS

The following instrument options are available.

- **Option 1, Rack Mounting**. Rack mount kit containing a set of track slides (90° tilt capability), mounting ears, and front panel handles for mounting the instrument in a standard 19-inch equipment rack.
- **Option 2A, 110 dB Step Attenuator**. Adds a 10 dB per step attenuator with a 110 dB range for models having a high-end frequency of ≤26 5 GHz. Output power is selected directly in dBm on the front panel (or via GPIB). Rated output power is reduced.
- **Option 2B, 110 dB Step Attenuator**. Adds a 10 dB per step attenuator with a 110 dB range for models having a high-end frequency of ≤40 GHz. Output power is selected directly in dBm on the front panel (or via GPIB). Rated output power is reduced.
- **Option 2C, 90 dB Step Attenuator.** Adds a 10 dB per step attenuator with a 90 dB range for models having a high-end frequency of ≤50 GHz. Output power is selected directly in dBm on the front panel (or via GPIB). Rated output power is reduced.
- **Option 2D, 90 dB Step Attenuator.** Adds a 10 dB per step attenuator with a 90 dB range for models having a high-end frequency of ≤60 GHz. Output power is selected directly in dBm on the front panel (or via GPIB). Rated output power is reduced.
- **Option 9, Rear Panel RF Output**. Moves the RF output connector to the rear panel.
- **Option 11, 0.1 Hz Frequency Resolution**. Provides frequency resolution of 0.1 Hz.
- **Option 14, ANRITSU 360B VNA Compatibility**. Modifies rack mounting hardware to mate unit in a ANRITSU 360B VNA console.
- **Option 15A, High Power Output**. Adds high-power RF components to the instrument in the 2–26.5 GHz frequency range. Option 15A is standard in models having a high-end frequency that is >40 GHz.
- **Option 16, High-Stability Time Base**. Adds an ovenized, 10 MHz crystal oscillator with $<5 \times 10^{-10}$/day frequency stability.

- **Options 17A & 17B, No Front Panel.** Deletes the front panel for use in remote control applications where a front panel display or keyboard control are not needed. Option 17A deletes the front panel from 691XXA models; Option 17B deletes the front panel from 690XXA models.
- **Option 18, mmWave Module Bias Output.** Provides bias output for 54000-xWRxx Millimeter Wave Source Modules. BNC Twinax connector, rear panel.
- **Option 19, SCPI Programmability.** Adds GPIB command mnemonics complying with Standard Commands for Programmable Instruments (SCPI), Version 1993. SCPI programming complies with IEEE 488.2-1987.

1-8 LEVEL OF MAINTENANCE

Maintenance of the 690XXA/691XXA consists of:

- Troubleshooting the instrument to a replaceable subassembly or RF component.
- Repair by replacing the failed subassembly or RF component.
- Calibration.
- Preventive maintenance.

Troubleshooting The 690XXA/691XXA firmware includes internal diagnostics that self-test most of the internal assemblies of the instrument. When the 690XXA/691XXA fails self-test, one or more error messages are displayed to aid in troubleshooting the failure to a replaceable subassembly or RF component. Chapter 5–Troubleshooting lists and describes the self-test error messages and provides procedures for isolating 690XXA/691XXA failures to a replaceable subassembly or RF component.

Repair Most instrument failures are field repairable by replacing the failed subassembly or RF component. Detailed instructions for removing and replacing failed subassemblies and components are provided in Chapter 6–Removal and Replacement Procedures.

Calibration The 690XXA/691XXA may require calibration after repair. Refer to Chapter 4–Calibration for a listing of calibration requirements and calibration procedures.

Preventive Maintenance Preventive maintenance on the 690XXA/691XXA consists of cleaning the fan honeycomb filter, described in paragraph 1-9.

1-9 PREVENTIVE MAINTENANCE

The 690XXA/691XXA must always receive adequate ventilation. A blocked fan filter can cause the instrument to overheat and shut down. Check and clean the rear panel fan honeycomb filter periodically. Clean the fan honeycomb filter more frequently in dusty environments. Clean the filter as follows.

Step 1 Remove the filter guard from the rear panel by pulling out on the four panel fasteners holding them in place (Figure 1-2).

Step 2 Vacuum the honeycomb filter to clean it.

Step 3 Install the filter guard back on the rear panel.

Step 4 Press in on the panel fasteners to secure the filter guard to the rear panel.

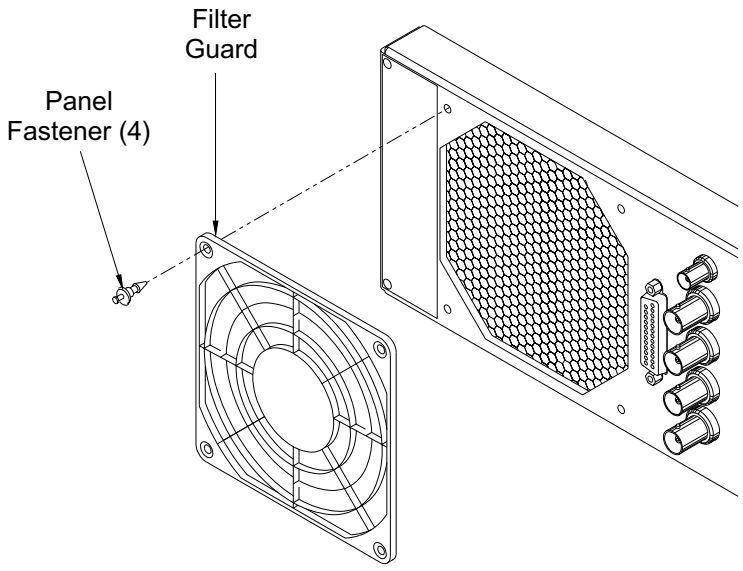


Figure 1-2. *Removing/Replacing the Fan Filter Guard*

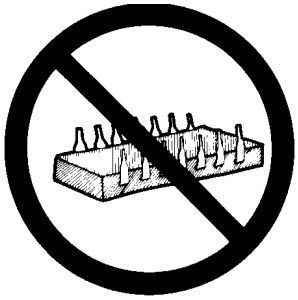
1-10 STATIC-SENSITIVE COMPONENT HANDLING PRECAUTIONS

The 690XXA/691XXA contains components that can be damaged by static electricity. Figure 1-3 illustrates the precautions that should be followed when handling static-sensitive subassemblies and components. If followed, these precautions will minimize the possibilities of static-shock damage to these items.

NOTE

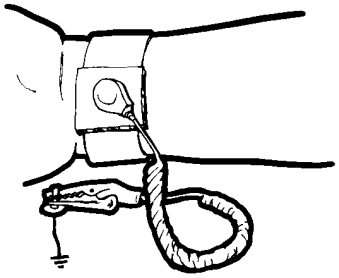
Use of a grounded wrist strap when removing and/or replacing subassemblies or components is strongly recommended.

1. Do not touch exposed contacts on any static sensitive component.



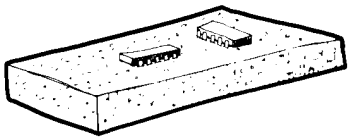
2 Do not slide static sensitive component across any surface.

3. Do not handle static sensitive components in areas where the floor or work surface covering is capable of generating a static charge.

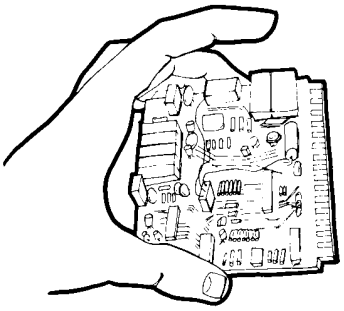


4. Wear a static-discharge wristband when working with static sensitive components.

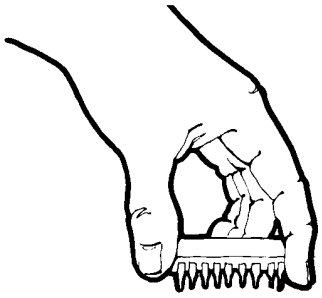
5. Label all static sensitive devices.



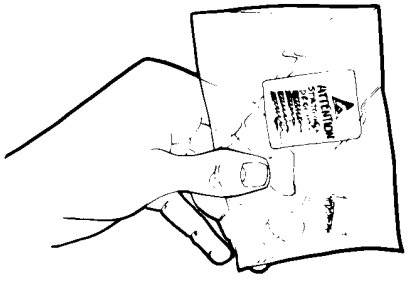
6. Keep component leads shorted together whenever possible.



7. Handle PCBs only by their edges. Do not handle by the edge connectors.



8. Lift & handle solid state devices by their bodies – never by their leads.



9. Transport and store PCBs and other static sensitive devices in static-shielded containers.

10. ADDITIONAL PRECAUTIONS:

- Keep workspaces clean and free of any objects capable of holding or storing a static charge.
- Connect soldering tools to an earth ground.
- Use only special anti-static suction or wick-type desoldering tools.

Figure 1-3. *Static-Sensitive Component Handling Precautions*

1-11 STARTUP CONFIGURATIONS

The 690XXA/691XXA comes from the factory with a jumper across pins 2 and 3 of front panel connector J12 (Figure 1-4). In this configuration, connecting the instrument to line power automatically places it in operate mode (front panel OPERATE LED on).

The startup configuration can be changed so that the 690XXA/691XXA comes up in standby mode (front panel STANDBY LED on) when it is connected to line power. Change the startup configuration as follows:

Step 1 Disconnect the instrument from line power.

Step 2 Remove the top cover from the 690XXA/691XXA. (Refer to Chapter 6 for instructions).

Step 3 Locate front panel connector J12 and remove the jumper from across pins 2 and 3. It is located on the A2A1 PCB which plugs into the Front Panel Assembly.

Step 4 Install the jumper across pins 1 and 2 of connector J12.

Step 5 Install the top cover and connect the 690XXA/691XXA to line power. The instrument should come up in standby mode.

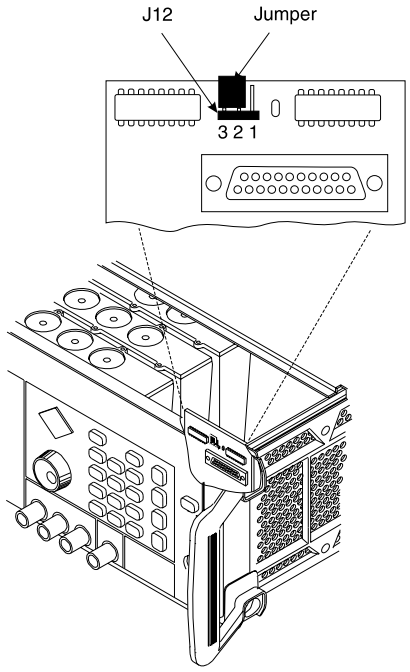


Figure 1-4. *Startup Configuration of Connector J12*

1-12 RECOMMENDED TEST EQUIPMENT

Table 1-2 provides a list of recommended test equipment needed for the performance verification, calibration, and troubleshooting procedures presented in this manual.

Table 1-2. *Recommended Test Equipment (1 of 2)*

INSTRUMENT	CRITICAL SPECIFICATION	RECOMMENDED MANUFACTURER/MODEL	USAGE (1)
Spectrum Analyzer, with External Mixers and Diplexer Assy	*Frequency Range:* 0.01 to 65 GHz *Resolution Bandwidth:* 10 Hz	Tektronix, Model 2794, with External Mixers: WM780K (18 to 26.5 GHz) WM780A (26.5 to 40 GHz) WM780U (40 to 60 GHz) WM780E (60 to 90 GHz) Diplexer Assy: 015-0385-00	C, P, T
Spectrum Analyzer	*Frequency Range:* 20 Hz to 40 MHz *Resolution Bandwidth:* 3 Hz	Hewlett-Packard, Model 3585B	P
Frequency Counter with Cable Kit and External Mixer	*Frequency Range:* 0.01 to 65 GHz *Input Impedance:* 50Ω *Resolution:* 1 Hz *Other:* External Time Base Input	EIP Microwave, Inc. Models 538B, 548B, or 578B, with Cable Kit: Option 590 and External Mixer: Option 91 (26.5 to 40 GHz) Option 92 (40 to 60 GHz) Option 93 (60 to 90 GHz)	C, P
Power Meter, with Power Sensor	*Power Range:* –30 to +20 dBm (1μW to 100mW)	Hewlett-Packard Model 437B, with Power Sensor: HP 8487A (0.01 to 50 GHz)	C, P
Power Meter, with Power Sensor	*Power Range:* –30 to +20 dBm (1μW to 100mW)	ANRITSU ML4803A, with Power Sensor: MP716A4 (50 to 75 GHz)	C,P
Digital Multimeter	*Resolution:* 4-1/2 digits (to 20V) *DC Accuracy:* 0.002% +2 counts *DC Input Impedance:* 10 MΩ *AC Accuracy:* 0.07% +100 counts (to 20 kHz) *AC Input Impedance:* 1 MΩ	John Fluke, Inc., Model 8840A, with Option 8840A-09K (True RMS AC)	C, T
Frequency Reference	*Frequency:* 10 MHz *Accuracy:* 5 x 10^{-12} parts/day	Absolute Time Corp., Model 300	P
Function Generator	*Output Voltage:* 2 volts peak-to-peak *Functions:* 0.4 Hz to 100 kHz sine and square waveforms	Hewlett-Packard, Model 8116A	C
Function Generator	*Output Voltage:* 2 volts peak-to-peak *Functions:* 0.4 Hz to 100 kHz sine and square waveforms	Hewlett-Packard, Model 33120A	C
Oscilloscope	*Bandwidth:* DC to 150 MHz *Vertical Sensitivity:* 2mV/division *Horizontal Sensitivity:* 50 ns/division	Tektronix, Inc. Model TAS485	P, T

Table 1-2. *Recommended Test Equipment (2 of 2)*

INSTRUMENT	CRITICAL SPECIFICATION	RECOMMENDED MANUFACTURER/MODEL	USAGE (1)
Mixer	*Frequency Range:* 1 to 26 GHz	Macom Micro Electronics Div. Model DMS1-26A	P
Scalar Network Analyzer, with RF Detector	*Frequency Range:* 0.01 to 60 GHz	ANRITSU, Model 562, with RF Detector: 560-7K50 (0.01 to 40 GHz) 560-7VA50 (0.01 to 50 GHz) SC5198 (40 to 60 GHz)	C, T
Adapter	K (male) to 2.4 mm (female) Adapts the Power Sensor, HP 8487A, to the 690XXA/691XXA RF OUTPUT connector (≤40 GHz models)	Hewlett-Packard Part Number: HP 11904D	C, P
Adapter	Adapts the MP716A4 Power Sensor to the ML4803A Power Meter	ANRITSU MA4002B	C, P
Adapter	WR15 to V (male) Adapts the MP716A4 Power Sensor to the 690XXA/691XXA RF OUTPUT connector (>40 GHz models)	ANRITSU, Model 35WR15V	C, P
Attenuator	*Frequency Range:* DC to 40 GHz *Max Input Power:* >+17 dBm *Attenuation:* 10 dB	ANRITSU, Model 41KC-10	C, P
Attenuator	*Frequency Range:* DC to 40 GHz *Max Input Power:* >+17 dBm *Attenuation:* 20 dB	ANRITSU, Model 41KC-20	P
Attenuator	*Frequency Range:* DC to 60 GHz *Max Input Power:* >+17 dBm *Attenuation:* 10 dB	ANRITSU, Model 41V-10	C, P
Attenuator	*Frequency Range:* DC to 60 GHz *Max Input Power:* >+17 dBm *Attenuation:* 20 dB	ANRITSU, Model 41V-20	P
RF Detector	*Frequency Range:* 0.01 to 40 GHz *Output Polarity:* Negative	ANRITSU, Model 75KC50 (K input/BNC output connectors)	T
RF Detector	*Frequency Range:* 0.01 to 50 GHz *Output Polarity:* Negative	ANRITSU, Model 75VA50 (V input/BNC output connectors)	T
Personal Computer	*PC Configuration:* IBM AT or compatible *Operating System:* Windows 3.1 *Accessories:* Mouse	Any common source	C
Serial Interface Assy	Provides serial interface between the PC and the 690XXA/691XXA.	ANRITSU P/N: T1678	C
Tee	*Connectors:* 50Ω BNC	Any common source	C, P
Cables	*Connectors:* 50Ω BNC	Any common source	C, P, T

NOTES: (1) P = Performance Verification Tests (Chapter 3); C = Calibration (Chapter 4); T = Troubleshooting (Chapter 5)

1-13 EXCHANGE ASSEMBLY PROGRAM

ANRITSU maintains an exchange assembly program for selected 690XXA/691XXA subassemblies and RF components. If a malfunction occurs in one of these subassemblies, the defective unit can be exchanged. Upon receiving your request, ANRITSU will ship the exchange subassembly or RF component to you, typically within 24 hours. You then have 45 days in which to return the defective item. All exchange subassemblies or RF components are warranted for 90 days from the date of shipment, or for the balance of the original equipment warranty, whichever is longer.

Please have the exact model number and serial number of your unit available when requesting this service, as the information about your unit is filed according to the instrument's model and serial number. For more information about the program, contact your local sales representative or call your local ANRITSU service center. Refer to Table 1-5, on page 1-18, for a list of current ANRITSU service centers.

1-14 REPLACEABLE SUBASSEMBLIES AND PARTS

Table 1-3, on page 1-15, lists those replaceable subassemblies and RF components of the 690XXA/691XXA that are presently covered by the ANRITSU exchange assembly program. Table 1-4, on page 1-16, lists common replaceable parts for the 690XXA/691XXA that are not presently on the exchange assembly program.

All parts listed in Tables 1-3 and 1-4 may be ordered from your local ANRITSU service center.

Table 1-3. *Replaceable Subassemblies and RF Components (1 of 2)*

SUBASSEMBLY OR PART NAME	ANRITSU PART NUMBER
Printed Circuit Board Assemblies	
Front Panel Assy 691XXA	ND40832
Front Panel Assy 690XXA	ND40514
A3 Reference Loop PCB Assy	D37436-4
A4 Coarse Loop PCB Assy	D40624-3
A5 Fine Loop PCB Assy	D40635-3
A5 Fine Loop PCB Assy (w/Option 11)	D40635-7
A6 Square Wave Generator PCB Assy	D37406-3
A7 YIG Loop PCB Assy	D40627-3
A9 PIN Control PCB Assy	D40639-3
A10 ALC PCB Assy (691XXA)	D40610-3
A10 ALC PCB Assy (690XXA)	D40610-4
A11 FM PCB Assy (691XXA)	D40641-3
A11 FM PCB Assy (690XXA)	D40641-5
A12 Analog Instruction PCB Assy	D37448-3
A13 YIG Driver PCB Assy	D40613-3
A14 SDM Driver PCB Assy 26.5 GHz	D40614-4
A14 SDM, SQM Driver PCB Assy	D40614-3
A15 Regulator PCB Assy	D40615-3
A16 CPU Interface PCB Assy	D37416-3
A17 CPU PCB Assy	D37444-3
A18 Power Supply PCB Assy	D40618-3
A19 Power Conditioner PCB Assy	D40619-3
A21 Line Filter/Rectifier PCB Assy	ND39918
A21-1 BNC/AUX I/O Connector PCB Assy 691XXA	ND39919
A21-2 BNC/AUX I/O Connector PCB Assy 690XXA	ND40528
10 MHz Crystal Oscillator Assy	D37332
RF Components	
YIG-Tuned Oscillator, 2 to 20 GHz	C27327
Down Converter	D27330
Digital Down Converter	D29450
Switched Doubler Module, 20 to 26.5 GHz	ND40843
Switched Doubler Module, 20 to 40 GHz	D28535
Source Quadrupler Module, 40 to 50 GHz	D28185
Source Quadrupler Module, 40 to 60 GHz	60-141
Source Quadrupler Module, 40 to 65 GHz	60-142
Coupler, 40 GHz	D27115
Coupler, 60 GHz	D27350

Table 1-3. *Replaceable Subassemblies and RF Components (2 of 2)*

SUBASSEMBLY OR PART NAME	ANRITSU PART NUMBER
RF Components (Continued)	
Forward Coupler, 60 GHz	C27184
Switched Filter	D29393
Switched Filter (w/Option 15A)	D29390
Output Connector Assy “K”	ND39077
Output Connector Assy “V”	ND40835
Step Attenuator, 110 dB, 26.5 GHz	D27152
Step Attenuator, 110 dB, 40 GHz	D25080
Step Attenuator, 90 dB, 50 GHz	D27315
Step Attenuator, 90 dB, 60 GHz	D28957

Table 1-4. *Common Replaceable Subassemblies and Parts (1 of 2)*

SUBASSEMBLY OR PART NAME	ANRITSU PART NUMBER
Cap, Protective (for RF Output K-Connector)	A20304
Cap, Protective (for RF Output V-Connector)	B37220
Cover, Top	D37131
Cover, Bottom	D37135
Cover, Side	D37133
Cover, Side Handle	761-67
Cover, CPU Housing	C37063
Cover, Main Card Cage	D37064
Cover, Power Supply Housing	C37062
EMI Gasket for side covers	790-437
EMI Gasket for side covers	790-390
EMI Gasket for Front Panel Assy	790-223
Fan Assembly	A40513
Fan Mount	790-425
Fan Membrane (Honey Comb Filter)	C37137
Fan Grill	790-426
Fasteners (for Fan Grill)	790-433
Fuse, 5A, 3AG Slow Blow (110 Vac)	631-33
Fuse, 2.5A, 3AG Slow Blow (230 Vac)	631-14
Gasket, RFI (“O”rings for MCX connectors)	790-393

Table 1-4. *Common Replaceable Subassemblies and Parts (2 of 2)*

SUBASSEMBLY OR PART NAME	ANRITSU PART NUMBER
Handle, Side Carrying	783-830
Screw, Handle Side Carrying	900-714
Line Module	260-11
Shield Cover	D37228
Shield	D37229
Standoff	785-922
Tape	850-70
Foot, Rear Bottom Left	2000-548
Foot, Rear Bottom Right	2000-549
Foot, Rear Top Left	2000-552
Foot, Rear Top Right	2000-553
Screw, Green Head	2000-560
690XXA/691XXA without Front Handles Installed	
Foot, Front Bottom Left	2000-546
Foot, Front Bottom Right	2000-547
Foot, Front Top Left	2000-550
Foot, Front Top Right	2000-551
690XXA/691XXA with Front Handles Installed	
Upper Insert	B37147
Foot, Bottom Left	C37170
Foot, Bottom Right	C37171
Handle, Left	D37168-2
Handle, Right	D37169-2
Tilt Bail	790-435

Table 1-5. *ANRITSU Service Centers*

UNITED STATES

ANRITSU COMPANY
490 Jarvis Drive
Morgan Hill, CA 95037-2809
Telephone: (408) 776-8300
1-800-ANRITSU
FAX: 408-776-1744

ANRITSU COMPANY
10 New Maple Ave., Unit 305
Pine Brook, NJ 07058
Telephone: (973) 227-8999
1-800-ANRITSU
FAX: 973-575-0092

ANRITSU COMPANY
1155 E. Collins Blvd
Richardson, TX 75081
Telephone: 1-800-ANRITSU
FAX: 972-671-1877

AUSTRALIA

ANRITSU PTY. LTD.
Unit 3, 170 Foster Road
Mt Waverley, VIC 3149
Australia
Telephone: 03-9558-8177
FAX: 03-9558-8255

BRAZIL

ANRITSU ELECTRONICA LTDA.
Praia de Botafogo, 440, Sala 2401
CEP22250-040, Rio de Janeiro, RJ, Brasil
Telephone: 021-527-6922
FAX: 021-53-71-456

CANADA

ANRITSU INSTRUMENTS LTD.
700 Silver Seven Road, Suite 120
Kanata, Ontario K2V 1C3
Telephone: (613) 591-2003
FAX: (613) 591-1006

CHINA

ANRITSU ELECTRONICS (SHANGHAI) CO. LTD.
2F, Rm B, 52 Section Factory Building
No. 516 Fu Te Rd (N)
Shanghai 200131 P.R. China
Telephone:21-58680226, 58680227, 58680228
FAX: 21-58680588

FRANCE

ANRITSU S.A
9 Avenue du Quebec
Zone de Courtaboeuf
91951 Les Ulis Cedex
Telephone: 016-09-21-550
FAX: 016-44-61-065

GERMANY

ANRITSU GmbH
Grafenberger Allee 54-56
D-40237 Dusseldorf, Germany
Telephone: 0211-968550
FAX: 0211-9685555

INDIA

MEERA AGENCIES PVT. LTD.
23 Community Centre
Zamroodpur, Kailash Colony Extension,
New Delhi, India 110 048
Phone: 011-2-6442700/6442800
FAX : 011-2-644250023

ISRAEL

TECH-CENT, LTD.
4 Raul Valenberg St
Tel-Aviv 69719
Telephone: (03) 64-78-563
FAX: (03) 64-78-334

ITALY

ANRITSU Sp.A
Roma Office
Via E. Vittorini, 129
00144 Roma EUR
Telephone: (06) 50-99-711
FAX: (06) 50-22-4252

KOREA

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Head Office:
14F, Hyunjuk Building 832-41
Yeoksam-Dong, Kangnam-Ku
Seoul 135-080, South Korea
Telephone: 02-553-6603
FAX: 02-553-6604

Service Center:
8F Hyunjuk Building
832-41, Yeoksam Dong
Kangnam-Gu
Seoul, South Korea 135-080
Telephone: 82-2-553-6603
FAX: 82-2-553-6605

JAPAN

ANRITSU CUSTOMER SERVICE LTD.
1800 Onna Atsugi-shi
Kanagawa-Prf. 243 Japan
Telephone: 0462-96-6688
FAX: 0462-25-8379

SINGAPORE

ANRITSU (SINGAPORE) PTE LTD.
10, Hoe Chiang Road
#07-01/02 Keppel Towers
Singapore 089315
Telephone: 282-2400
FAX: 282-2533

SOUTH AFRICA

ETECSA
12 Surrey Square Office Park
330 Surrey Avenue
Ferndale, Randburt, 2194
South Africa
Telephone: 011-27-11-787-7200
FAX: 011-27-11-787-0446

SWEDEN

ANRITSU AB
Botivid Center
Fittja Backe 13A
145 84 Stockholmn
Telephone: (08) 534-707-00
FAX: (08) 534-707-30

TAIWAN

ANRITSU CO., INC.
7F, No. 316, Section 1
NeiHu Road
Taipei, Taiwan, R.O.C.
Telephone: 886-2-8751-1816
FAX: 886-2-8751-2126

UNITED KINGDOM

ANRITSU LTD.
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Luton, Bedfordshire
LU1 3LU, England
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Chapter 2
Functional Description

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Table of Contents (Continued)

Chapter 2
Functional Description

2-1 INTRODUCTION

This chapter provides brief functional descriptions of the major subsystems that are contained in each model of the Series 690XXA/691XXA Synthesized CW/Sweep Generators. In addition, the operation of the frequency synthesis, automatic level control (ALC), and RF deck subsystems is described so that the reader may better understand the overall operation of the instrument. Block diagrams are included to supplement the written descriptions.

2-2 690XXA/691XXA MAJOR SUBSYSTEMS

The 690XXA/691XXA circuitry consists of various distinct subsystems that are contained on one or more printed circuit board (PCB) assemblies or in microwave components located on the RF deck. The following paragraphs identify the subsystems that make up the instrument and provide a brief description of each. Figure 2-1 (page 2-6) is an overall block diagram of a typical 690XXA/691XXA.

NOTE

Although identical model numbers of the series 690XXA CW generators and series 691XXA sweep generators contain the same major subsystems, there are some functional differences between them. These functional differences result fromthe series 691XXA having the additional capability of producing analog frequency sweeps and AM, FM, and square wave modulation of the RF output signal. Functional differences between the series are noted in the following descriptions where applicable.

Digital Control

This circuit subsystem consists of the A17 CPU and A16 CPU Interface PCBs. The central processor unit (CPU) is the main controller for the 690XXA/691XXA. This controller directly or indirectly controls all functions of the instrument. The CPU contains memory that stores the main operating system components and instrument firmware, instrument calibration data, and front panel setups in the power-off condition. It has a GPIB interface that allows it to communicate with external devices over the GPIB and a serial interface to a serial terminal port on the rear panel. The CPU is directly linked via a dedicated data and address bus to the A2 Front Panel PCB, the A9 PIN Control PCB, the A10 ALC PCB, the A11 FM PCB, the A12 Analog Instruction PCB, and the A16 CPU Interface PCB.

The CPU is indirectly linked via the A16 CPU Interface PCB to the A3 Reference Loop PCB, the A4 Coarse Loop PCB, the A5 Fine Loop PCB, and the A6 Square Wave Generator PCB. The A16 PCB contains circuitry to perform parallel-to-serial and serial-to-parallel data conversion. It also contains circuitry for many of the rear panel signals, a 13-bit resolution DVM, and decoder circuitry for the front panel rotary data knob optical encoder.

Front Panel

This circuit subsystem consists of the the A1 Front Panel PCB, the A2 Front Panel Control PCB, and the Liquid Crystal Display (LCD). This subsystem interfaces the front panel LCD, LEDs, and keys to the CPU via the dedicated data and address bus. The front panel rotary data knob is indirectly linked to the CPU via the A16 CPU Interface PCB.

The A1 Front Panel PCB contains the keyboard matrix of conductive rubber switches. The A2 Front Panel Control PCB has circuits to control the LCD dot-matrix display, turn the front panel LEDs on and off, and convert keyboard switch matrix signals to parallel keycode. It also contains the standby/operate line switch logic circuit and the optical encoder for the rotary data knob.

Frequency Synthesis

The frequency synthesis subsystem consists of the A3 Reference Loop PCB, the A4 Coarse Loop PCB, the A5 Fine Loop PCB, the A7 YIG Loop PCB, and the A11 FM PCB. It provides the reference frequencies and phase lock circuits for precise control of the YIG-tuned oscillator frequencies, as follows:

- The A3 Reference Loop PCB supplies the stable 10 MHz, 100 MHz, and 500 MHz reference frequency signals for the rest of the frequency synthesis system.
- The A4 Coarse Loop PCB generates coarse tuning frequencies of 202.5 to 990 MHz for use by the YIG Loop.
- The A5 Fine Loop PCB provides fine tuning frequencies of 30 to 40 MHz for use by the YIG Loop.
- The A7 YIG Loop PCB performs phase detection of the YIG-tuned oscillator's output frequency and provides a YIG loop error voltage to the A11 PCB.
- The A11 FM PCB conditions the YIG loop error voltage, producing a correction signal that is

used to fine tune and phase lock the YIG-tuned oscillator. In the 691XXA, the A11 PCB also contains circuitry for frequency modulation of the YIG-tuned oscillator RF output.

The CPU sends control data to the A3 Reference Loop PCB, the A4 Coarse Loop PCB, and the A5 Fine Loop PCB via the A16 PCB as serial data words. The CPU controls the A11 FM PCB via the dedicated data and address bus. Refer to paragraph 2-3 for a functional overview of the frequency synthesis subsystem.

Analog Instruction

The A12 Analog Instruction PCB provides the frequency tuning voltages and frequency band select signals to the A13 YIG Driver PCB. For models with a frequency range greater than 20 GHz, it supplies frequency band select signals to the A14 SDM, SQM Driver PCB. In addition, it provides a 0V to +10V ramp signal to the rear panel HORIZ OUT connector, a V/GHz signal to the rear panel V/GHz OUT connector, and a SLOPE signal to the A10 ALC PCB for slope-vs-frequency correction of the RF output power. The A17 CPU controls the A12 Analog Instruction PCB via the dedicated data and address bus.

YIG Driver

The A13 YIG Driver PCB supplies the tuning current and bias voltages for the 2 to 20 GHz YIG-tuned oscillator. It also provides bias voltages for the Down Converter assembly and the amplifiers located in the Switched Filter assembly.

The A12 Analog Instruction PCB provides (1) frequency tuning voltages for the main tuning coil driver of the YIG-tuned oscillator and (2) frequency band select signals to activate the appropriate bias voltage supply.

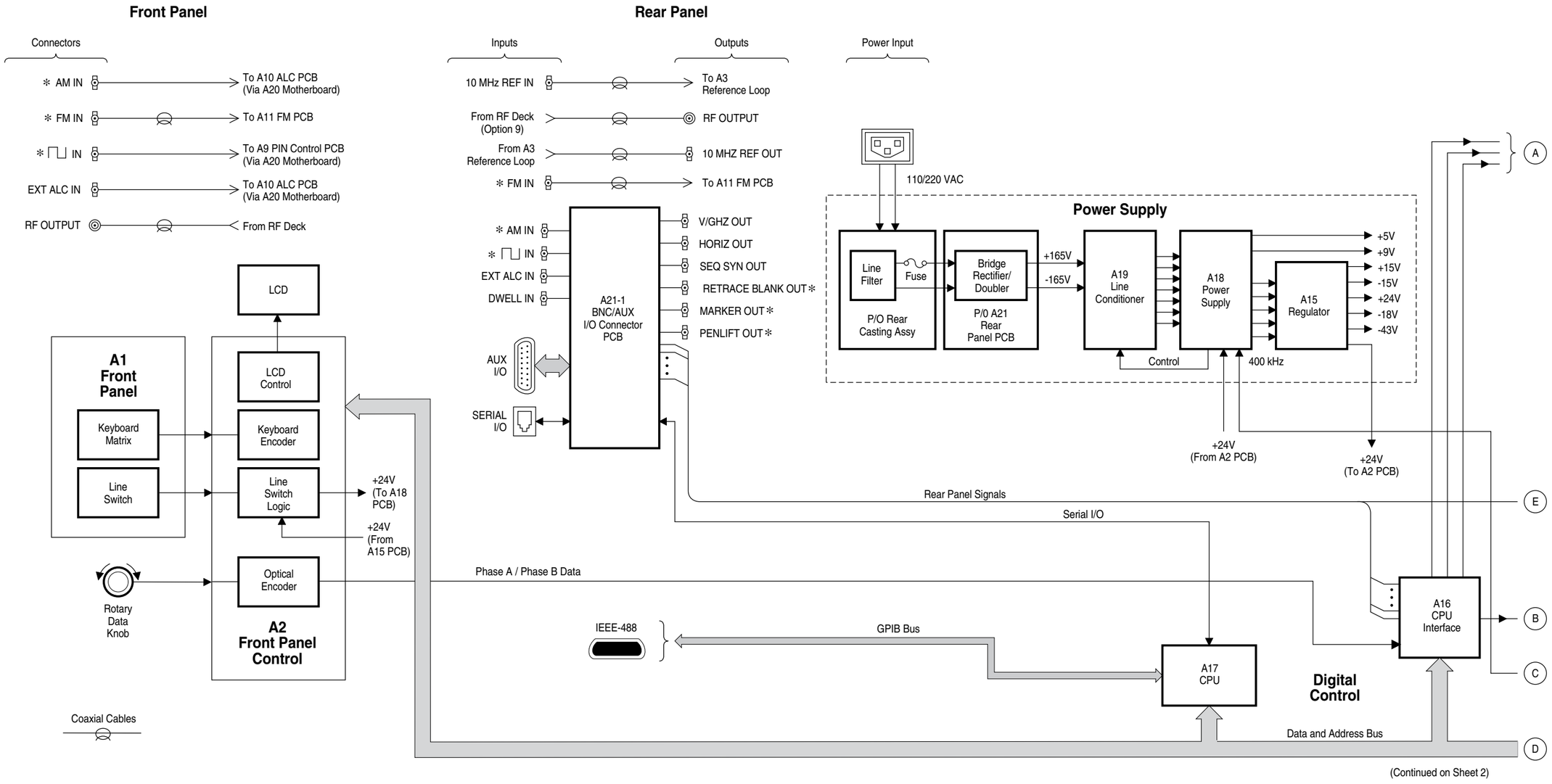


Figure 2-1. Block Diagram of a Typical 690XXA/691XXA Synthesized CW/Sweep Generator (Sheet 1 of 2)

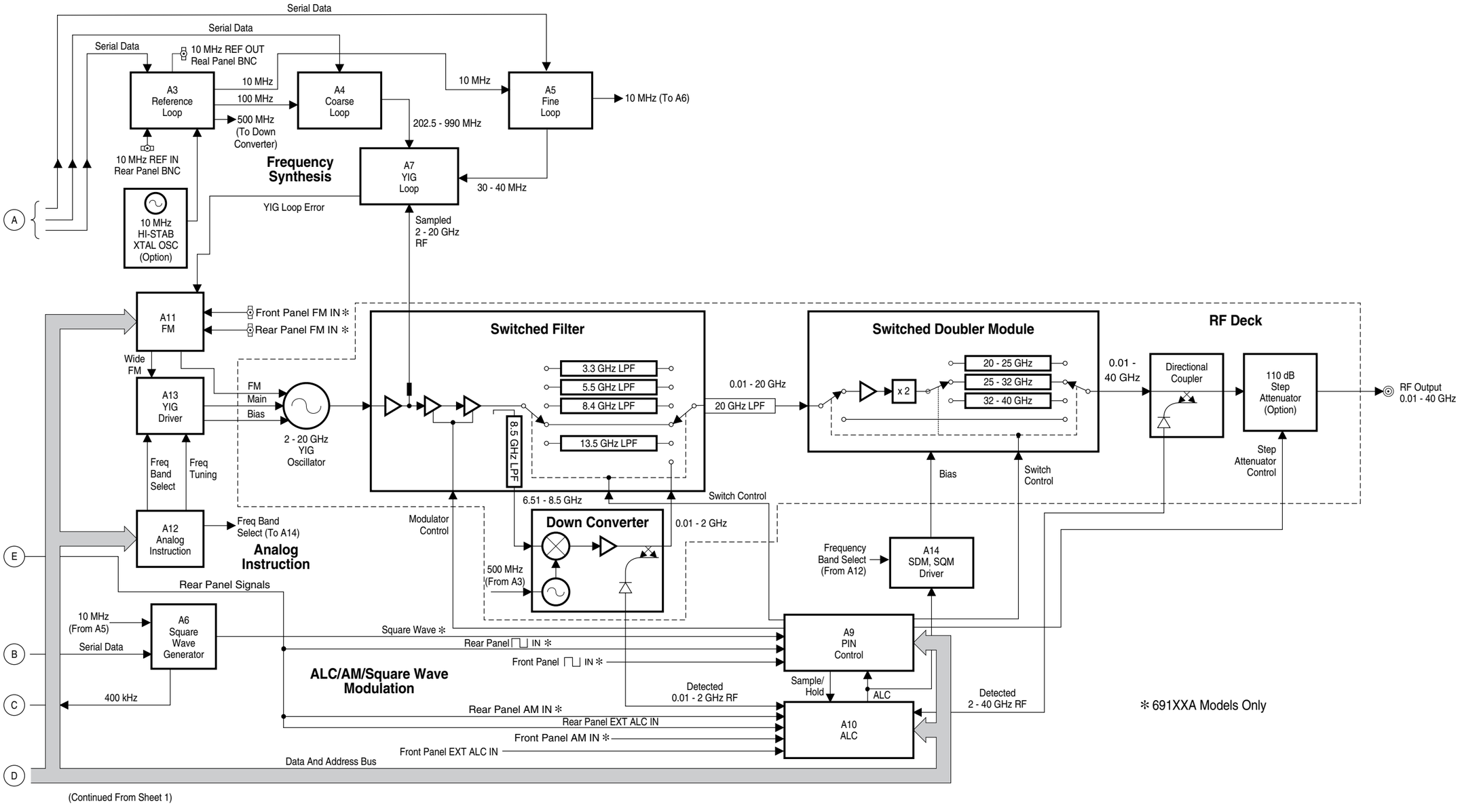


Figure 2-1. Block Diagram of a Typical 690XXA/691XXA Synthesized CW/Sweep Generator (Sheet 2 of 2)

ALC/ Modulation

This circuit subsystem consists of the A6 Square Wave Generator PCB, the A9 PIN Control PCB, the A10 ALC PCB, and the A14 SDM, SQM Driver PCB. It provides the following:

- Level control of the RF output power.
- In the 691XXA, AM modulation and square wave modulation.
- Current drive signals to the PIN switches located in the Switched Filter assembly and Switched Doubler Module (SDM).
- Bias voltages for the Switched Doubler Module and Source Quadrupler Module (SQM).
- Drive signals for the optional Step Attenuator.

The A17 CPU controls the A9 Pin Control PCB and the A10 ALC PCB via the dedicated data and address bus. It sends control data to the A6 Square Wave Generator PCB via the A16 PCB as serial data words. Refer to paragraph 2-4 for a functional overview of the ALC and modulation subsystem.

RF Deck

This subsystem contains those elements related to the generation, modulation, and control of the sweep- and CW-frequency RF signals. These elements include; the 2 to 20 GHz YIG-tuned oscillator, the 0.01 to 2 GHz (0.5 to 2.2 GHz) Down Converter assembly, the Switched Filter assembly, the Switched Doubler Module (SDM), the Source Quadrupler Module (SQM), the Directional Coupler/Level Detector, and the optional 110 dB (90 dB) Step Attenuator. Refer to paragraph 2-5 for a functional overview of the RF deck subsystem.

Power Supply

The power supply subsystem consists of the A15 Regulator PCB, the A18 Power Supply PCB, the A19 Line Conditioner PCB, and part of the A21 Rear Panel PCB and Rear Casting Assembly. It supplies all the regulated DC voltages used by the 690XXA/691XXA circuits. The voltages are routed throughout the instrument via the A20 Motherboard PCB.

Inputs/ Outputs

The A21-1 BNC/AUX I/O Connector PCB and the A16 CPU Interface PCB contain the interface circuits for the majority of the rear panel input and output connectors, including the AUX I/O connector.

The front panel external ALC input goes via the A20 Motherboard PCB to the A10 ALC PCB; the rear

panel external ALC input routes by way of the A21-1 PCB and the A20 PCB to the A10 PCB. The rear panel connectors, 10 MHz REF OUT and 10 MHz REF IN, are coupled directly to the A3 Reference Loop PCB via coaxial cables. The rear panel IEEE-488 GPIB and SERIAL I/O connectors are connected to the A17 CPU PCB by way of the Motherboard PCB.

In 691XXA models, the front panel AM and Square Wave inputs go by way of the Motherboard PCB to the internal PCBs—the AM input to the A10 ALC PCB and the Square Wave input to the A9 PIN Control PCB. The rear panel AM and Square Wave inputs route via the A21-1 PCB and the Motherboard PCB to their respective internal PCBs. The front panel and rear panel FM inputs are coupled directly via coaxial cable to the A11 FM PCB.

Motherboard/ Interconnections

The A20 Motherboard PCB and associated cables provide the interconnections for the flow of data, signals, and DC voltages between all internal components and assemblies throughout the 690XXA/ 691XXA.

2-3 FREQUENCY SYNTHESIS

The frequency synthesis subsystem provides phase-lock control of the 690XXA/691XXA output frequency. It consists of four phase-lock loops, the Reference Loop, the Coarse Loop, the Fine Loop, and the YIG Loop. The four phase-lock loops, operating together, produce an accurately synthesized, low-noise RF output signal. Figure 2-2 (page 2-11) is an overall block diagram of the frequency synthesis subsystem. The following paragraphs describe phase-lock loops and the overall operation of the frequency synthesis subsystem.

Phase Lock Loops

The purpose of a phase-lock loop is to control the frequency of a variable oscillator in order to give it the same accuracy and stability as a fixed reference oscillator. It works by comparing two frequency inputs, one fixed and one variable, and supplying a correction signal to the variable oscillator to reduce the difference between the two inputs. For example, suppose we have a 10 MHz reference oscillator with a stability of 1×10^{-7}/day, and we wish to transfer that stability to a voltage controlled oscillator (VCO). The 10 MHz reference signal is applied to the reference input of a phase-lock loop circuit. The signal from the VCO is applied to the variable input. A phase detector in the phase-lock loop circuit compares the two inputs and determines whether the

variable input waveform is leading or lagging the reference. The phase detector generates a correction signal that (depending on polarity) causes the VCO frequency to increase or decrease to reduce any phase difference. When the two inputs match, the loop is said to be *locked*. The variable input from the VCO then equals the reference input in phase, frequency, accuracy, and stability.

In practical applications a frequency divider is placed between the output of the variable oscillator and the variable input to the phase-lock loop. The circuit can then be used to control a frequency that is an exact multiple of the reference frequency. In this way, the variable oscillator acquires the stability of the reference without equaling its frequency. In the A3 Reference Loop, the 100 MHz oven-controlled crystal oscillator (OCXO) can be controlled by the phase-lock loop using a 10 MHz reference. This is because a divide-by-ten circuit is between the OCXO's output and the variable input to the phase-lock loop. Both inputs to the phase detector will be 10 MHz when the loop is locked.

If a programmable frequency divider is used, a number of frequencies can be phase-locked to the same reference. The limitation is that all must be exact multiples of the reference. The A4 Coarse Loop and A5 Fine Loop both use programmable frequency dividers.

Overall Operation

The YIG-tuned oscillator generates a high-power RF output signal that has low broadband noise and low spurious content. The frequency of the YIG-tuned oscillator is controlled by means of (1) its main tuning coil and (2) its FM (fine tuning) coil. Main tuning coil current from the YIG Driver PCB coarsely tunes the YIG-tuned oscillator to within a few megahertz of the final output frequency. The YIG phase-lock loop is then used to fine tune the YIG-tuned oscillator to the exact output frequency and to reduce FM noise close to the carrier.

One input to the YIG Loop is the 202.5 to 990 MHz signal from the Coarse Loop. This signal is amplified to drive the step-recovery diode. The step-recovery diode produces harmonics of the coarse loop signal (≥1.9625 to 20.04 GHz). These harmonics are used by the sampler.

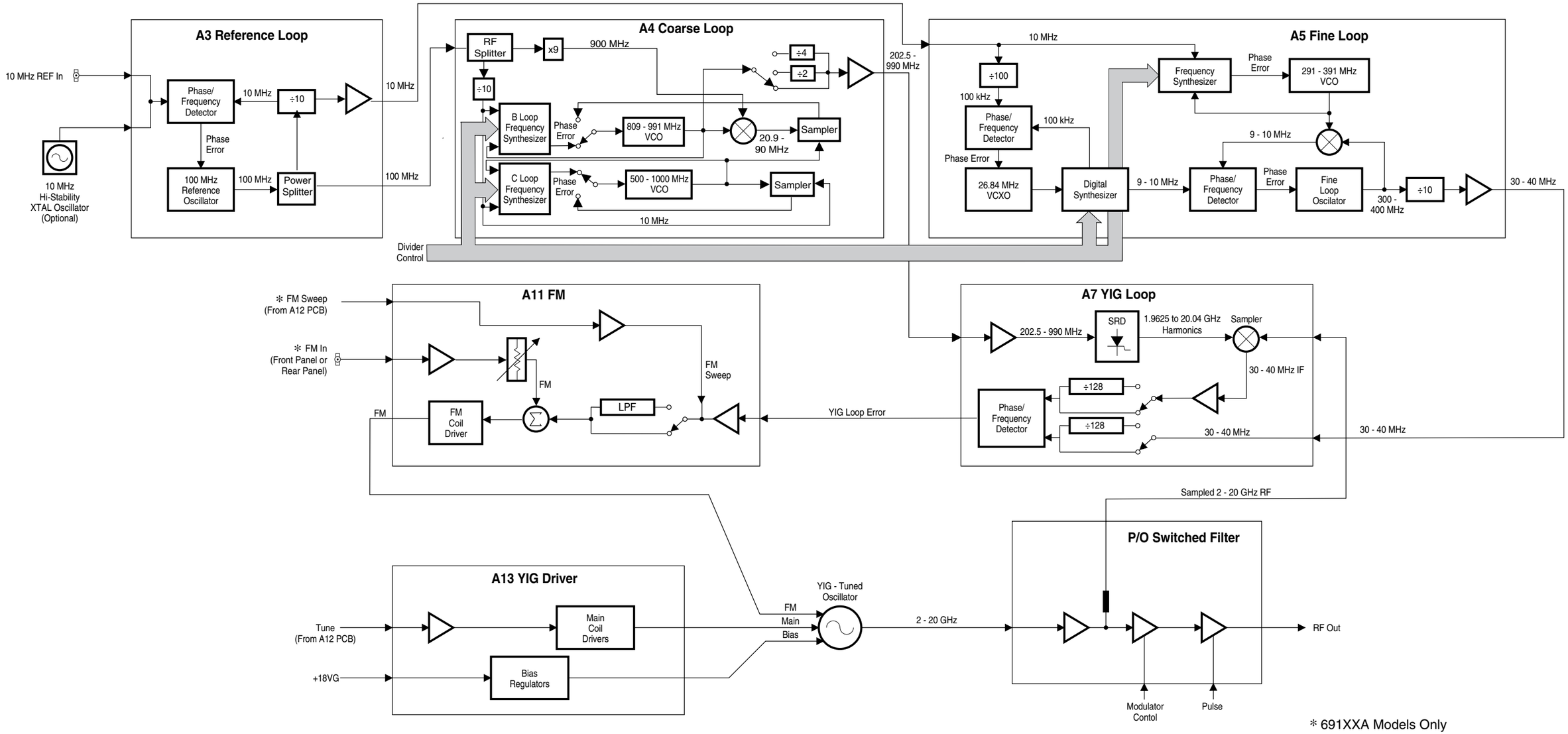


Figure 2-2. Block Diagram of the Frequency Synthesis Subsystem

The other input to the sampler is the RF output signal from the YIG-tuned oscillator. Mixing this RF output signal sample with the adjacent coarse-loop harmonic produces a low frequency difference signal that is the YIG IF signal (30 to 40 MHz).

The 690XXA/691XXA CPU programs the coarse-loop oscillator's output frequency so that one of its harmonics will be within 30 to 40 MHz of the desired YIG-tuned oscillator's output frequency. The YIG Loop phase detector compares the YIG IF signal to the 30 to 40 MHz reference signal from the Fine Loop. If there is a difference, the YIG phase detector fine tunes the YIG-tuned oscillator (via the FM circuitry and the FM coil drivers) to eliminate any frequency difference between the two signals.

Phase locking the instrument's output frequency over a broad frequency range is accomplished by programming the coarse-loop oscillator's output to various frequencies that have harmonics close to the desired operating frequencies. Exact frequency tuning for each desired operating frequency is accomplished by programming the fine-loop oscillator. (In each case, the YIG-tuned oscillator is first tuned via the main tuning coil to the approximate desired operating frequency.) Table 2-1 shows the coarse-loop and fine-loop frequencies for some specific RF output frequencies.

Table 2-1. *RF Output and Loop Frequencies*

RF OUTPUT/LOOP FREQUENCIES (in MHz)		
RF OUT	**COARSE LOOP**	**FINE LOOP**
2000	218.055	37.5
3000	217.143	40.0
4000	212.631	40.0
5000	402.000	40.0
6000	464.615	40.0
7000	469.333	40.0
8000	472.941	40.0
9000	821.818	40.0
10000	836.667	40.0
11000	849.231	40.0
12000	926.154	40.0

The coarse-loop oscillator has a programming (tuning) range of 202.5 to 990 MHz. This provides harmonics from ≥1.9625 GHz to 20.04 GHz. This allows any YIG-tuned oscillator output frequency to be down converted to a YIG IF signal of 21.5 to 40 MHz.

The YIG Loop is fine tuned by varying the 30 to 40MHz reference signal applied to the YIG loop phase detector. By programming the fine-loop oscillator, this signal can be adjusted in 1 kHz increments over the 30 to 40 GHz range. The resolution of the fine-loop oscillator (hence the resolution of the RF output signal) is 1 kHz, which is much finer than is available from the coarse loop alone. For applications requiring a resolution finer than 1 kHz, an optional tuning resolution of 0.1 Hz is available.

The Coarse Loop and Fine Loop outputs are derived from high-stability 10 MHz and 100 MHz signals

generated by the Reference Loop. For applications requiring even greater stability, the 100 MHz reference oscillator can be phase locked to an optional 10 MHz reference (internal or external).

RF Outputs 0.01 to 65 GHz

Refer to the block diagram of the RF Deck shown in Figure 2-1 (page 2-7) for the following description. The 690XXA/691XXA uses one 2 to 20 GHz YIG-tuned oscillator. All other frequencies output by the instrument are derived from the fundamental frequencies generated by this YIG-tuned oscillator.

0.01 to 2 GHz

RF output frequencies of 0.01 to 2 GHz are developed by down converting the fundamental frequencies of 6.51 to 8.5 GHz. This is achieved using a 6.5 GHz local oscillator signal that is phase locked to the 500 MHz output of the Reference Loop. Precise control of the 0.01 to 2 GHz frequencies to 1 kHz (0.1 Hz with Option 11) accuracy is accomplished by phase-lock control of the 6.51 to 8.5 GHz fundamental frequencies prior to down conversion.

20 to 40 GHz

RF output frequencies of 20 to 40 GHz are produced by doubling the 10 to 20 GHz fundamental frequencies. Phase-lock control of the 10 to 20 GHz fundamental frequencies—accomplished prior to doubling—ensures precise control of the 20 to 40 GHz frequencies to 1 kHz (0.1 Hz with Option 11) resolution.

40 to 65 GHz

RF output frequencies of 40 to 65 GHz are developed by quadrupling of the 10 to 16.25 GHz fundamental frequencies (refer to Figure 2-5, page 2-22). Precise control of the 40 to 65 GHz to 1 kHz (0.1 Hz with Option 11) resolution is accomplished by phase-lock control of the 10 to 16.25 GHz fundamental frequencies prior to quadrupling.

0.5 to 2.2 GHz

RF output frequencies of 0.5 to 2.2 GHz for the 690X5A/691X5A models are developed by down converting the fundamental frequencies of 2 to 4.4 GHz (refer to Figure 2-6, page 2-27). Phase-lock control of the 2 to 4.4 GHz fundamental frequencies, achieved prior to down converting, ensures precise control of the 0.5 to 2.2 GHz frequencies to 1 kHz (0.1 Hz with Option 11) resolution.

Frequency Modulation (691XXA only)

Frequency modulation (FM) of the YIG-tuned oscillator RF output by external signals is performed by summing the external modulating signal into the FM control path of the YIG loop. Refer to Figures 2-1 and 2-2. The external modulating signal comes from the front panel or rear panel FM IN input. Circuits on the A11 FM PCB adjust the modulating signal for the proper amount of FM for the sensitivity selected, then sum it into the YIG loop FM control path. There, it frequency modulates the RF output signal by controlling the YIG-tuned oscillator's FM (fine tuning) coil current.

Analog Sweep Mode (691XXA only)

Broad-band analog frequency sweeps (>100 MHz wide) of the YIG-tuned oscillator RF output are accomplished by applying appropriate analog sweep ramp signals, generated by the A12 Analog Instruction PCB, to the YIG-tuned oscillator's main tuning coil (via the A13 YIG Driver PCB). In this mode, the start, stop, and bandswitching frequencies are phase-lock-corrected during the sweep.

NOTE

For 691X5A models at frequencies of ≤2.2 GHz, broad-band analog frequency sweeps are >25 MHz wide; narrow-band analog frequency sweeps are ≤25 MHz.

Narrow-band analog frequency sweeps (≤100 MHz wide) of the YIG-tuned oscillator RF output are accomplished by summing appropriate analog sweep ramp signals, generated by the A12 Analog Instruction PCB, into the YIG-tuned oscillator's FM tuning coil control path. The YIG-tuned oscillator's RF output is then swept about a center frequency. The center frequency is set by applying a tuning signal (also from the A12 PCB) to the YIG-tuned oscillator's main tuning coil (via the A13 YIG Driver PCB). In this mode, YIG loop phase locking is disabled except during center frequency correction, which occurs during sweep retrace.

Step Sweep Mode

Step (digital) frequency sweeps of the YIG-tuned oscillator RF output consist of a series of discrete, synthesized steps between a start and stop frequency. Each frequency step is generated by applying the tuning signal (from the A12 Analog Instruction PCB) to the YIG-tuned oscillator's main tuning coil, then phase-locking the RF output. Every frequency step in the sweep range is phase-locked.

2-4 ALC AND MODULATION

The ALC and modulation subsystem provides automatic level control (ALC), and in the 691XXA, amplitude modulation (AM) and square wave modulation of the RF output signal. The ALC loop consists of circuits located on the A10 ALC PCB, the A9 PIN Control PCB, and the A14 SDM, SQM Driver PCB. These circuits interface with the Switched Filter assembly, the Down Converter assembly, the Source Quadrupler Module (SQM), and the Directional Coupler/Level Detector (all located on the RF deck). AM modulation circuits (located on the A10 ALC PCB) are included in this loop.

Square wave modulation of the RF output signal is provided by circuits located on the A6 Square Wave Generator PCB and the A9 PIN Control PCB. The overall block diagram of the ALC and modulation subsystem is shown in Figure 2-3, page 2-17. The following paragraphs describe the operation of the subsystem components.

ALC Loop Operation

In the 690XXA/691XXA, a portion of the RF output is detected and coupled out of the Directional Coupler/Level Detector as the feedback input to the ALC loop. The feedback signal from the detector is routed to the A10 ALC PCB where it is compared with a *reference voltage* that represents the desired RF power output level. If the two voltages do not match, an error correction signal is fed from the A10 ALC PCB to the modulator shaper amplifier circuits located on the A9 PIN Control PCB and the A14 SDM, SQM Driver PCB, if installed. The resulting ALC control voltage output causes the modulator, located in the Switched Filter assembly, the SQM, and the Digital Down Converter assembly (690X5A/691X5A models only) to adjust the RF output level. Thus, the feedback signal from the detector will be set equal to the reference voltage.

NOTE

The instrument uses two internal level detection circuits. For frequencies <2 GHz (≤2.2 GHz for 690X5A/691X5A models), the level detector is part of the Down Converter. The signal from this detector is routed to the A10 ALC PCB as the Detector 0 input. For frequencies ≥2 GHz (>2.2 GHz for 690X5A/691X5A models), the level detector is part of the main Directional Coupler. The signal from this detector is routed to the A10 ALC PCB as the Detector 1 input.

The Level Reference DAC, under the control of the CPU, provides the RF level reference voltage. By setting the output of this DAC to the appropriate voltage, the CPU adjusts the RF output power to the level selected by the user. Leveled output power can be set over a maximum range of up to 28 dB (up to 131 dB with the optional 110 dB step attenuator) using front panel controls or the GPIB. Instruments with Option 15A (High Power) provide leveled output power over a maximum range of up to 22 dB (up to 125 dB with the optional 110 dB step attenuator).

External Leveling
In the external leveling mode, an external detector or power meter monitors the RF output level of the 690XXA/691XXA instead of an internal level detector. The signal from the external detector or power meter goes to the A10 ALC PCB from the front or rear panel inputs. The ALC controls the RF power output level as previously described.

ALC Slope
During analog sweeps (691XXA only), a slope-vs-frequency signal, from the A12 Analog Instruction PCB, is summed with the level reference and detector inputs into the ALC loop. The Slope DAC, under the control of the CPU, adjusts this ALC slope signal to compensate for an increasing or decreasing output power-vs-frequency characteristic caused by the level detectors and (optional) step attenuator. In addition (in both the 690XXA and the 691XXA), the Slope DAC lets the user adjust for the slope-vs-frequency characteristics of external components.

Power Sweep
In this mode, the CPU has the ALC step the RF output through a range of levels specified by the user. This feature can be used in conjunction with the sweep mode to produce a set of identical frequency sweeps, each with a different RF power output level.

Amplitude Modulation (691XXA only)

Amplitude modulation (AM) of the RF output signal by an external signal is accomplished by summing the external modulating signal into the ALC loop. External modulating signals come from the front panel or rear panel AM IN inputs. On the A10 PCB, the AM Input Sensitivity DAC and the AM Calibration DAC, under the control of the CPU, adjust the modulating signal for the proper amount of AM in both the linear (log amp in) and the log (log amp

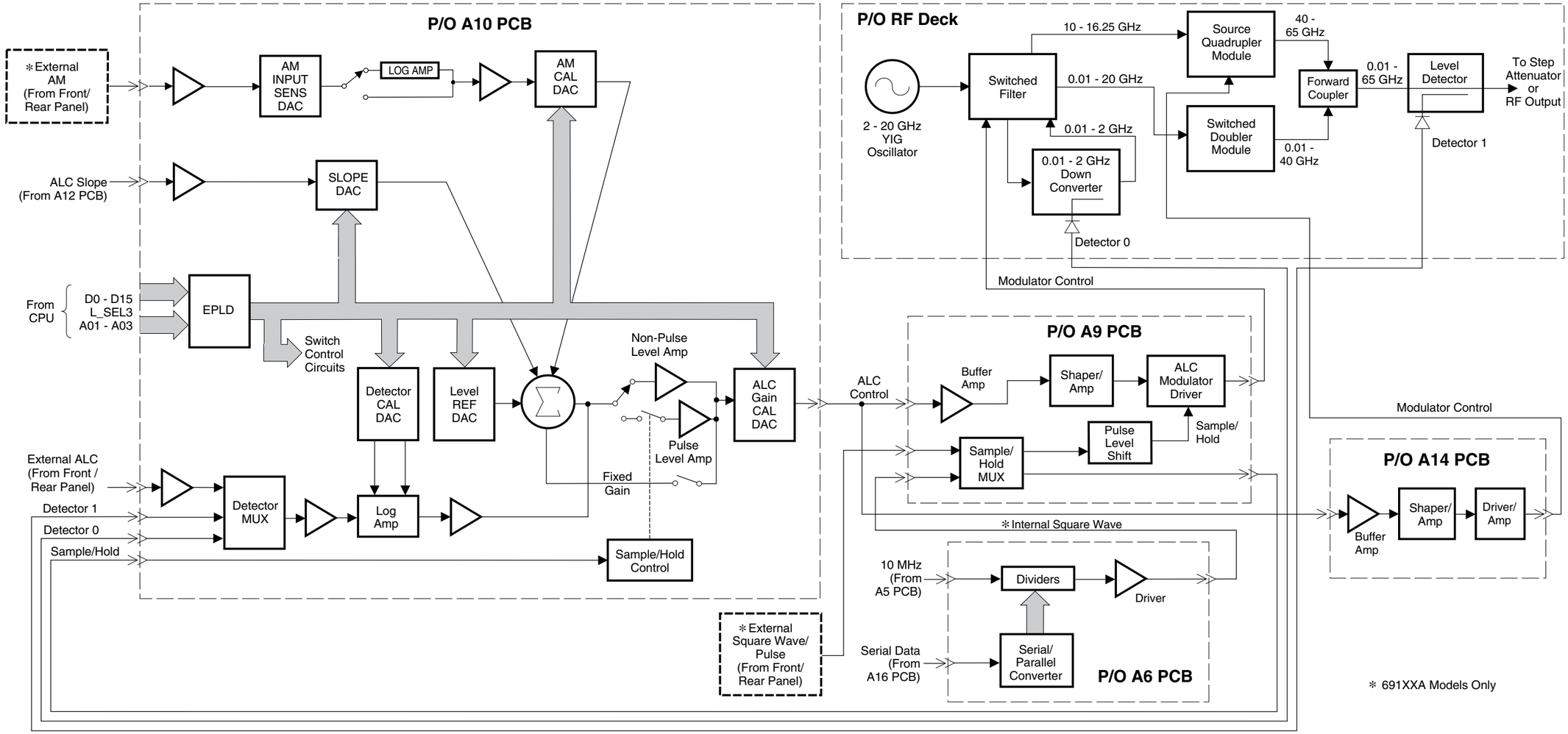


Figure 2-3. Block Diagram of the ALC and Modulation Subsystem

out) modes of operation. The adjusted modulating signal is summed with the level reference, slope, and detector inputs into the ALC loop. This produces an ALC control signal that varies with the modulating signal. The action of the ALC loop then causes the envelope of the RF output signal to track the external modulation signal.

Square Wave Modulation (691XXA only)

Square wave modulation is accomplished by turning the RF output signal on and off using internally generated square wave or external square wave inputs.

The A6 Square Wave Generator PCB, under control of the CPU, divides the 10 MHz reference signal received from the A5 Fine Loop PCB to produce square waves. These internal square wave signals are fed to the A9 PIN Control PCB. There they are multiplexed with the external square wave signals received from the front or rear panel. The output of the multiplexer is two sample/hold signals. One goes via a pulse level shift circuit to the ALC modulator driver to modulate the RF output signal; the other goes to the A10 ALC PCB to cause the level amplifier to operate as a sample/hold amplifier. The amplifier is synchronized with the modulating signal so that the ALC loop effectively operates only during the *ON* portion of the modulated RF output signal.

2-5 RF DECK ASSEMBLIES

The primary purpose of the RF deck assembly is to generate CW and swept frequency RF signals and route these signals to the front panel RF OUTPUT connector. It is capable of generating RF signals in the frequency range of 0.01 to 65 GHz.

The series 690XXA/691XXA synthesized CW/sweep generators use a single 2 to 20 GHz YIG-tuned oscillator. All other frequencies are derived from the fundamental frequencies generated by this oscillator, as follows:

- RF output frequencies of 0.01 to 2 GHz are developed by down-converting the fundamental frequencies of 6.51 to 8.5 GHz.
- RF output frequencies of 0.5 to 2.2 GHz are developed by down-converting the fundamental frequencies of 2 to 4.4 Ghz.
- RF output frequencies of 20 to 40 GHz are produced by doubling the fundamental frequencies of 10 to 20 GHz.
- RF output frequencies of 40 to 65 GHz are produced by quadrupling the fundamental frequencies of 10 to 16.25 GHz.

The following paragraphs briefly describe the operation of the RF deck assembly.

RF Deck Configurations

All 690XXA/691XXA RF deck assemblies contain a 2 to 20 GHz YIG-tuned oscillator, a switched filter assembly, and a directional coupler. Beyond that, the configuration of the RF deck assembly varies according to the particular instrument model. Block diagrams of the various RF deck configurations are shown in the following figures:

- Figure 2-4, page 2-21, is a block diagram of the RF deck assembly for all ≤40 GHz models except for 690X5A/691X5A models.
- Figure 2-5, page 2-22, is a block diagram of the RF deck assembly for all >40 GHz models except for 690X5A/691X5A models.
- Figure 2-6, page 2-27, is a block diagram of the RF deck assembly for all ≤40 GHz 690X5A/691X5A models.
- Figure 2-8, page 2-28, is a block diagram of the RF deck assembly for all >40 GHz 690X5A/691X5A models.

The block diagram of the RF deck shown in Figure 2-4 (page 2-21) includes all of the common RF components found in the 690XXA/691XXA RF deck assemblies. Refer to this block diagram during the descriptions of RF deck operation presented in the following paragraphs.

YIG-tuned Oscillator

The 2 to 20 GHz YIG-tuned oscillator actually contains two oscillators—one covering the frequency range of 2 to 8.4 GHz and one covering the frequency range of 8.4 to 20 GHz. Both oscillators use a common internal amplifier.

The YIG-tuned oscillator generates RF output signals that have low broadband noise and low spurious content. It is driven by the Main tuning coil current and bias voltages from the A13 YIG Driver PCB and the FM tuning coil current from the A11 FM PCB. During CW mode, the main tuning coil current tunes the oscillator to within a few megahertz of the final output frequency. The phase-lock circuitry of the YIG loop then fine adjusts the oscillator's FM tuning coil current to make the output frequency exact. In the 691XXA, frequency modulation of the RF output is also accomplished by sum-

ming the external modulating signals into the oscillator's FM tuning coil control path.

When the 691XXA is generating broad-band analog frequency sweeps (>100 MHz wide), the main tuning coil current tunes the oscillator through the sweep frequency range. Phase locking to fine adjust the oscillator's output frequency is only done at the bottom and top of the sweep ramp and on both sides of each band switch point. Narrow-band analog frequency sweeps (≤100 MHz wide) in the 691XXA are accomplished by summing the appropriate sweep ramp signal into the oscillator's FM tuning coil control path. The YIG-tuned oscillator's RF output is then swept about a center frequency that is set by the main tuning coil current. Phase locking to fine tune the output frequency is done at the center frequency of the sweep.

NOTE

For 691X5A models at frequencies of ≤2.2 GHz, broad-band analog frequency sweeps are >25 MHz wide; narrow-band analog frequency sweeps are ≤25 MHz.

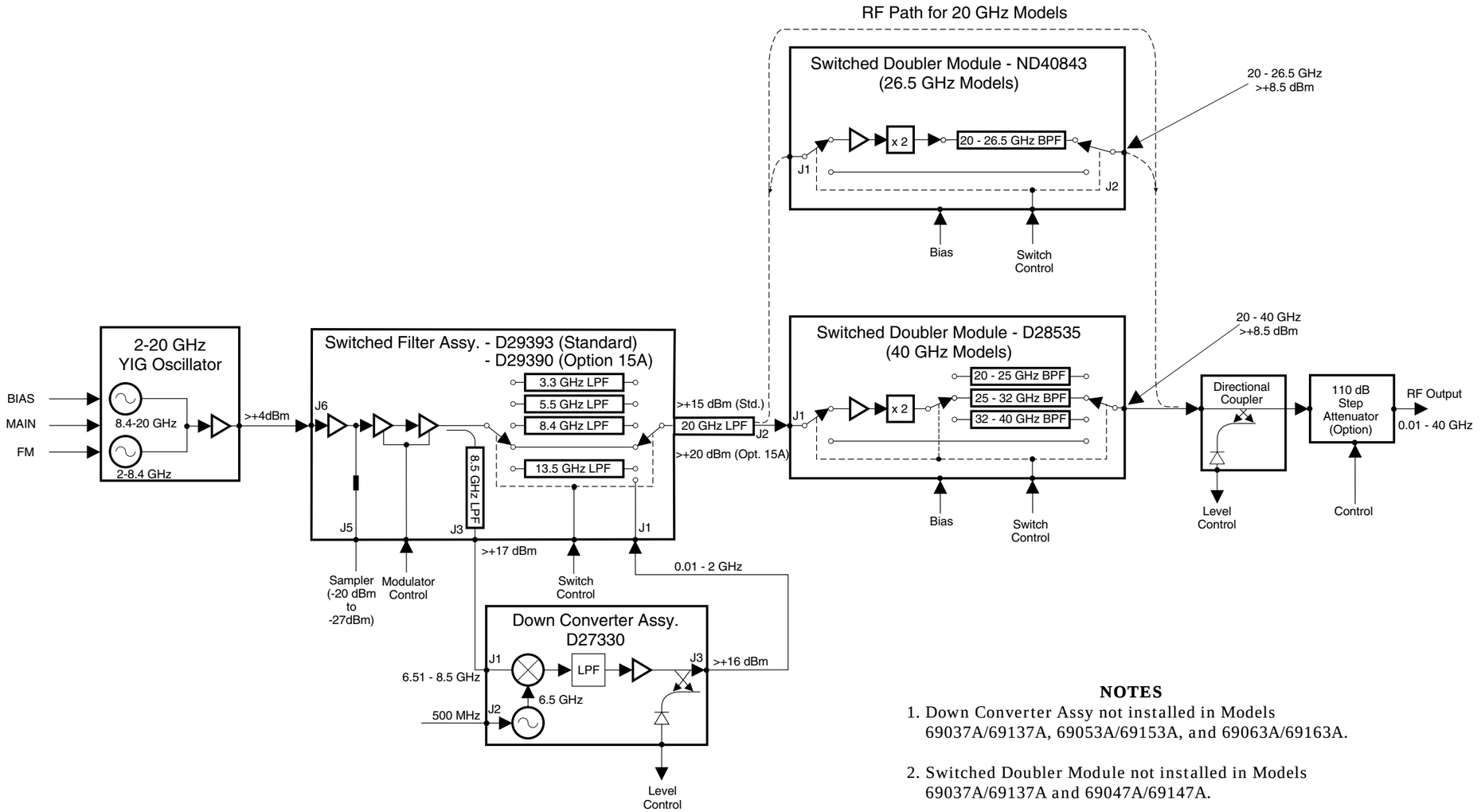
Power Level Control and Modulation

The RF output signal from the YIG-tuned oscillator goes to connector J6 on the switched filter assembly. In the switched filter assembly, the RF signal is amplified then goes to the modulator. A portion of the RF signal to the modulator is picked off and coupled out via connector J5 to the Sampler for use by the YIG loop circuitry. The modulator provides power level control and, in the 691XXA, AM and square wave modulation.

The modulator control signal is received from the A9 PIN Control PCB where it is developed from the ALC control signal. The modulator control signal adjusts the gain of the modulator to control the power level of the RF output signals. In the 691XXA, the modulator is also used for AM and square wave modulation of the RF output signals. Amplitude modulation is accomplished by varying the modulator control signal with the modulating signal. Square wave modulation is achieved by switching the modulator on and off at a rate determined by the modulating square wave.

RF Signal Filtering

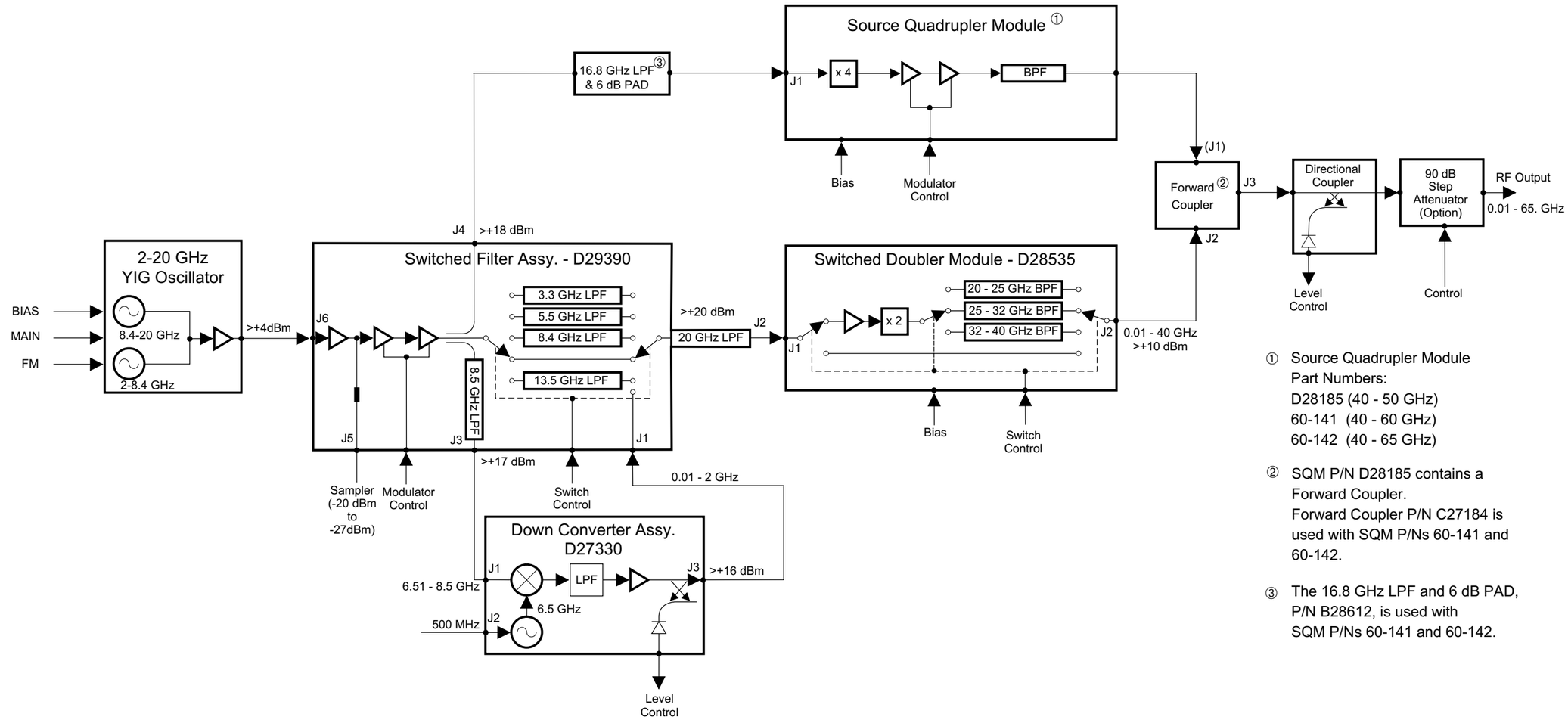
The RF signal from the modulator is routed via PIN switches to the switched low-pass filters. PIN switch drive current is received from the A9 PIN Control PCB. A coupler in the switched filter path provides the RF signal for the down converter. Whenever an instrument is generating RF signals of <2 GHz (≤2.2 GHz for 690X5A/691X5A models), a RF signal is coupled out, through a 8.5 GHz low-pass filter



NOTES

1. Down Converter Assy not installed in Models 69037A/69137A, 69053A/69153A, and 69063A/69163A.
2. Switched Doubler Module not installed in Models 69037A/69137A and 69047A/69147A.

Figure 2-4. Block Diagram of the RF Deck Assembly for all ≤40 GHz Models (except 690X5A/691X5A Models)



① Source Quadrupler Module Part Numbers:
D28185 (40 - 50 GHz)
60-141 (40 - 60 GHz)
60-142 (40 - 65 GHz)

② SQM P/N D28185 contains a Forward Coupler.
Forward Coupler P/N C27184 is used with SQM P/Ns 60-141 and 60-142.

③ The 16.8 GHz LPF and 6 dB PAD, P/N B28612, is used with SQM P/Ns 60-141 and 60-142.

Figure 2-5. Block Diagram of the RF Deck Assembly for all >40 GHz Models (except 690X5A/691X5A Models)

and connector J3 to the down converter. Another coupler in the switched filter path of high power switched filter assemblies provides the RF signal for the source quadrupler module (refer to Figure 2-5). Whenever an instrument is generating RF signals of >40 GHz, a RF signal is coupled out via J4 to the source quadrupler module.

The switched low-pass filters provide rejection of the harmonics that are generated by the YIG-tuned oscillator. The 2 to 20 GHz (>2.2 to 20 GHz for 690X5A/691X5A models) RF signal from the modulator has four filtering paths and a through path. The four filtering paths are 3.3 GHz, 5.5 GHz, 8.4 GHz, and 13.5 GHz. Signals above 13.5 GHz are routed via the through path.

After routing through the appropriate path, the 2 to 20 GHz (>2.2 to 20 GHz for 690X5A/691X5A models) RF signal is multiplexed by the PIN switches and goes via a 20 GHz low-pass filter to the switched filter assembly output connector J2. The 0.01 to 2 GHz (0.5 to 2.2 GHz for 690X5A/691X5A models) RF signal, from the down converter, is received at connector J1, then multiplexed through to the switched filter output.

From J2, the RF signal goes to either the directional coupler (≤20 GHz models) or the input connector J1 on the switched doubler module (>20 GHz models).

0.01 to 2 GHz Down Converter

The 0.01 to 2 GHz Down Converter assembly (Figures 2-4 and 2-5) contains a 6.5 GHz VCO that is phase-locked to the 500 MHz reference signal from the A3 Reference Loop PCB. The 6.5 GHz VCO's phase-lock condition is monitored by the CPU. The 6.5 GHz VCO is on at all times; however, the down converter amplifier is powered on by the A13 YIG Driver PCB only when the 0.01 to 2 GHz frequency range is selected.

During CW or swept frequency operations in the 0.01 to 2 GHz frequency range, the 6.51 to 8.5 GHz RF signal output from J3 of the switched filter assembly goes to input connector J1 of the down converter. The 6.51 to 8.5 GHz RF signal is then mixed with the 6.5 GHz VCO signal resulting in a 0.01 to 2 GHz RF signal. The resultant RF signal is fed through a 2 GHz low-pass filter, then amplified and routed to the output connector J3. A portion of the

down converter's RF output signal is detected, amplified, and coupled out for use in internal leveling. The detected RF sample is routed to the A10 ALC PCB.

The 0.01 to 2 GHz RF output from the down converter goes to input connector J1 of the switched filter assembly. There, the 0.01 to 2 GHz RF signal is multiplexed into the switched filter's output path.

0.5 to 2.2 GHz Digital Down Converter

The 0.5 to 2.2 GHz Digital Down Converter assembly (Figures 2-9 and 2-10), found in the 690X5A/691X5A models, provides improved phase noise across the 0.5 to 2.2 GHz frequency range. Power is applied to the down converter assembly at all times; however, the down converter amplifier is powered on by the A13 YIG Driver PCB only when the 0.5 to 2.2 GHz frequency range is selected.

During CW or swept frequency operations in the 0.5 to 2.2 GHz frequency range, the 2 to 4.4 GHz RF signal output from J3 of the switched filter assembly goes to the input connector J1 of the digital down converter. In the down converter, the 2 to 4.4 GHz RF signal is divided by 2 to produce frequencies of 1 to 2.2 GHz and divided by 2 again to develop frequencies of 0.5 to 1 GHz. From the frequency dividers, the 0.5 to 2.2 GHz RF signal then goes to the modulator which provides power level control.

The modulator control signal is received from the from the A9 PIN Control PCB where it is developed from the ALC control signal. The modulator control signal adjusts the gain of the modulator to control the power level of the RF output signals. In the 691XXA, the modulator is also used for AM and square wave modulation of the RF output signals. Amplitude modulation is accomplished by varying the modulator control signal with the modulating signal. Square wave modulation is achieved by switching the modulator on and off at a rate determined by the modulating square wave.

The RF signals from the modulator are amplified and fed via PIN switches to the switched low-pass filters. PIN switch drive current is generated by internal drivers that are controlled by signals received from the A12 Analog Instruction PCB. The switched low-pass filters provide rejection of unwanted har-

monics. The 0.5 to 2.2 GHz RF signal has four filter paths—700 MHz, 1000 MHz, 1400 MHz, and 2200 MHz. After routing through the appropriate filter path, the 0.5 to 2.2 GHz goes to connector J2. A portion of the down converter's RF output signal is detected, amplified, and coupled out for use in internal leveling. The detected RF sample is routed to the A10 ALC PCB.

The 0.5 to 2.2 GHz RF output from the down converter goes to input connector J1 of the switched filter assembly. There, the 0.5 to 2.2 GHz RF signal is multiplexed into the switched filter's output path.

Switched Doubler Module

The switched doubler module (SDM), found in >20 GHz models is used to double the fundamental frequencies of 10 to 20 GHz to produce RF output frequencies of 20 to 40 GHz.

26.5 GHz Models

The RF signal from the switched filter assembly is input to the SDM at J1. During CW or swept frequency operations in the 20 to 26.5 GHz frequency range, the 10 to 13.25 GHz RF signal input is routed by PIN switches to the doubler/amplifier. PIN switch drive current is provided by the A9 PCB and bias voltage for the doubler/amplifier is supplied by the A14 SDM,SQM Driver PCB. The RF signal is amplified, then doubled in frequency. From the doubler, the 20 to 26.5 GHz RF signal goes to the bandpass filter. After passing through the bandpass filter, the 20 to 26.5 GHz RF signal is multiplexed by the PIN switches to the SDM output at connector J2. RF signals input to the SDM of ≤20 GHz are multiplexed through by the PIN switches to output connector J2.

40 GHz Models

The RF signal from the switched filter assembly is input to the SDM at J1. During CW or swept frequency operations in the 20 to 40 GHz frequency range, the 10 to 20 GHz RF signal input is routed by PIN switches to the doubler/amplifiers. PIN switch drive current is provided by the A9 PCB and bias voltage for the doubler/amplifiers is supplied by the A14 SDM, SQM Driver PCB. The RF signal is amplified, then doubled in frequency. From the doubler, the 20 to 40 GHz RF signal is routed by PIN switches to the bandpass filters. There are three bandpass filter paths to provide good harmonic per-

formance. The frequency ranges of the three paths are 20 to 25 GHz, 25 to 32 GHz, and 32 to 40 GHz.

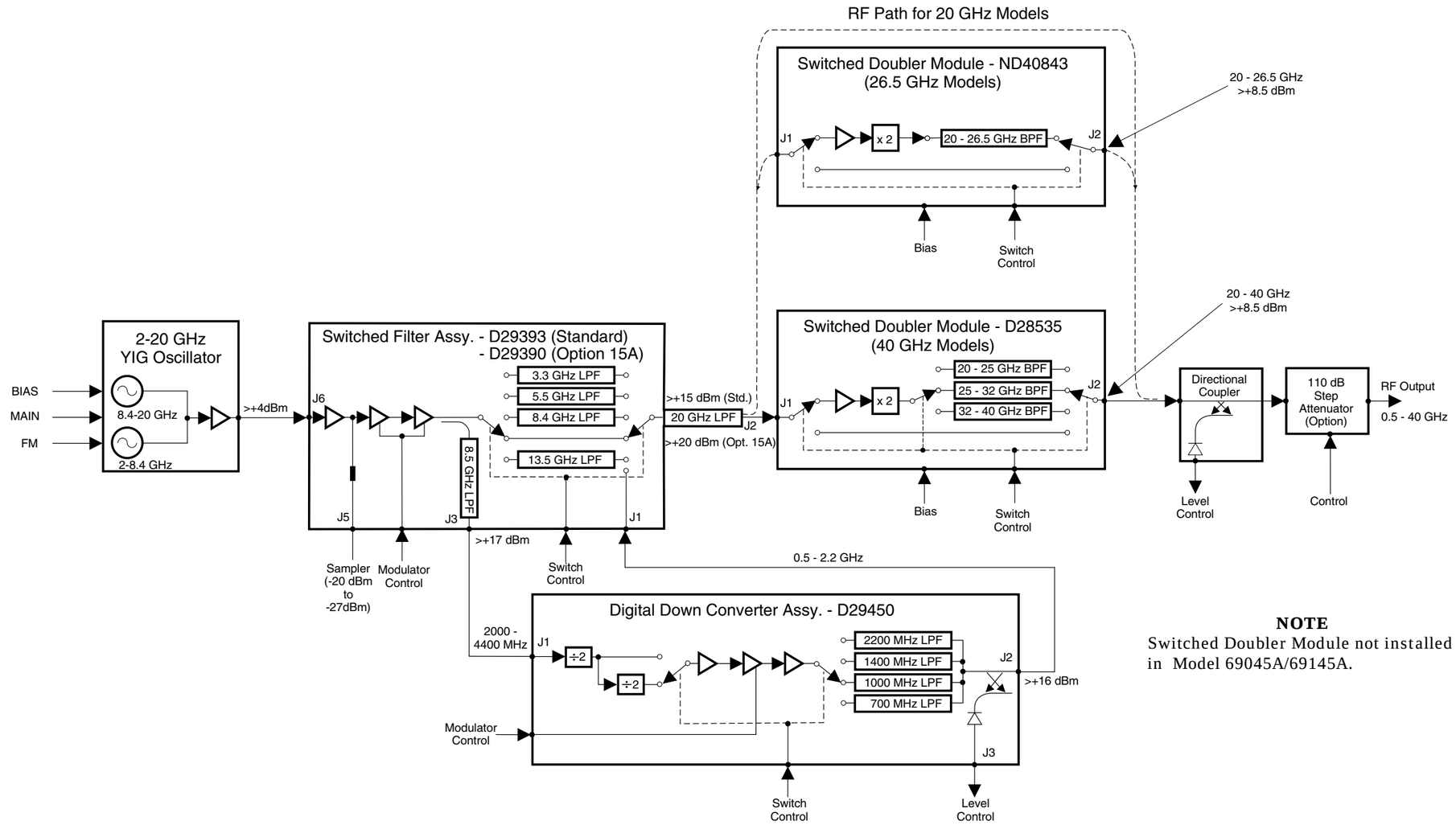
After routing through the appropriate bandpass filter path, the 20 to 40 GHz RF signal is multiplexed by the PIN switches to the SDM output at connector J2. RF signals input to the SDM of ≤20 GHz are multiplexed through by the PIN switches to output connector J2.

Source Quadrupler Module

The source quadrupler module (SQM), found in >40 GHz models, is used to quadruple the fundamental frequencies of 10 to 16.25 GHz to produce RF output frequencies of 40 to 65 GHz. The RF signal inputs for the SQM come from the switched filter assembly. The modulator control signal for the SQM is received from the A14 SDM, SQM Driver PCB where it is developed from the ALC control signal. The A14 PCB also supplies the amplifier bias voltage(s) for the SQM.

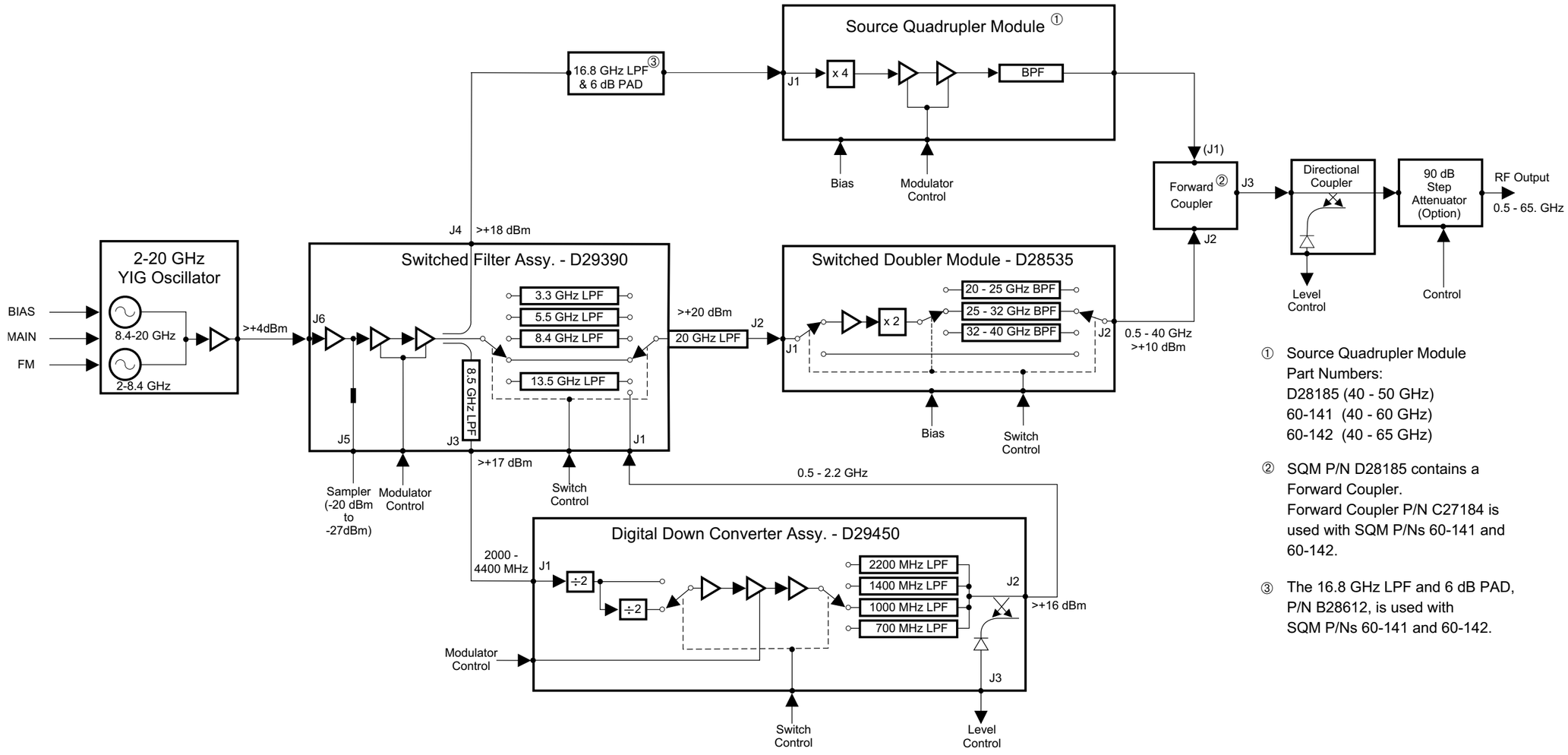
50 GHz Models (SQM P/N D28185)
During CW and swept frequency operations in the 40 to 50 GHz frequency range, the 10 to 12.5 GHz RF signal input is quadrupled and amplified, then goes to the modulator. The modulator provides for power level control and, in the 691XXA, amplitude modulation of the RF output signals. From the modulator, the 40 to 50 GHz RF signals goes via a band-pass filter to output connector J3 of the forward coupler. Note that on the 40 to 50 GHz SQM (P/N D28185), the forward coupler is an integral part of the SQM. The 0.01 to 40 GHz (0.5 to 40 GHz for 690X5A/691X5A models) RF output signals from the SDM are routed to input connector J2 of the SQM forward coupler. The 0.01 to 50 GHz (0.5 to 50 GHz for the 690X5A/691X5A models) RF output signals go from J3 of the SQM forward coupler to the directional coupler.

60 GHz Models (SQM P/N 60-141)
During CW or swept frequency operations in the 40 to 60 GHz frequency range, the 10 to 15 GHz RF signal input is quadrupled and amplified, then goes to the modulator. The modulator provides for power level control and, in the 691XXA, amplitude modulation of the RF output signal. From the modulator, the 40 to 60 GHz RF signals go via a band-pass filter to the output connector of the SQM.



NOTE
Switched Doubler Module not installed in Model 69045A/69145A.

Figure 2-6. Block Diagram of the RF Deck Assembly for all ≤40 GHz 690X5A/691X5A Models



① Source Quadrupler Module Part Numbers:
D28185 (40 - 50 GHz)
60-141 (40 - 60 GHz)
60-142 (40 - 65 GHz)

② SQM P/N D28185 contains a Forward Coupler.
Forward Coupler P/N C27184 is used with SQM P/Ns 60-141 and 60-142.

③ The 16.8 GHz LPF and 6 dB PAD, P/N B28612, is used with SQM P/Ns 60-141 and 60-142.

Figure 2-7. Block Diagram of the RF Deck Assembly for all >40 GHz 690X5A/691X5A Models

From the SQM, the 40 to 60 GHz RF output signals go to the input connector J1 of the forward coupler, P/N C27184. The other input to the forward coupler at connector J2 is the 0.01 to 40 GHz (0.5 to 40 GHz for 690X5A/691X5A models) RF output signals from the SDM. From forward coupler output connector J3, the 0.01 to 60 GHz (0.5 to 60 GHz for 690X5A/691X5A models) RF output signals go to the directional coupler.

65 GHz Models (SQM P/N 60-142)
During CW or swept frequency operations in the 40 to 65 GHz frequency range, the 10 to 16.25 GHz RF signal input is qaudrupled and amplified, then goes to the modulator. The modulator provides for power level control and, in the 691XXA, amplitude modulation of the RF output signals. From the modulator, the 40 to 65 GHz RF signals go via a band-pass filter to the output connector of the SQM.

From the SQM, the 40 to 65 GHz RF output signals go to the input connector J1 of the forward coupler, P/N C27184. The other input to the forward coupler at connector J2 is the 0.01 to 40 GHz (0.5 to 40 GHz for 690X5A/691X5A models) RF output signals from the SDM. From forward coupler output connector J3, the 0.01 to 40 GHz (0.5 to 40 GHz for 690X5A/691X5A models) RF output signals go to the directional coupler.

Power Level Detection/ ALC Loop

The RF output signal from either the switched filter assembly (≤20 GHz models), the SDM (≤26.5 GHz or ≤40 GHz models), or forward coupler (>40 GHz models) goes to the directional coupler for transfer to the RF OUTPUT connector. A portion of the RF output signal is detected and coupled out as feedback to the ALC circuitry on the A10 ALC PCB. In these circuits, the signal from the detector is summed with the reference voltage that represents the desired RF output power level. The resulting voltage is fed from the A10 PCB to the ALC modulator driver circuit on the A9 PIN Control PCB (and the ALC modulator driver circuit on the A14 SDM, SQM Driver PCB for >40 GHz models). The modulator control signals go to the modulators in the switched filter assembly, the SQM (for >40 GHz models), and the digital down converter assembly (for 690X5A/691X5A models) to adjust the RF output power level.

Step Attenuator

The optional step attenuator provides up to 110 dB (90 dB for 50 GHz and 60 GHz models) attenuation of the RF output in 10 dB steps. The step attenuator drive current is supplied by the A9 Control PCB.

Chapter 3
Performance Verification

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Table of Contents (Continued)

Chapter 3
Performance Verification

3-1 INTRODUCTION

This chapter contains tests that can be used to verify the performance of the Series 690XXA/691XXA Synthesized CW/Sweep Generators to specifications. These tests support all instrument models having any version of firmware. Units with Option 2A, 2B, 2C, or 2D (110 dB or 90 dB step attenuators), Option 11 (0.1 Hz frequency resolution), and Option 15A (high power output) are also covered.

3-2 RECOMMENDED TEST EQUIPMENT

Table 3-1 (page 3-4) provides a list of the recommended test equipment for the performance verification tests.

The test procedures refer to specific test equipment front panel control settings when the test setup is critical to making an accurate measurement. In some cases, the user may substitute test equipment having the same critical specifications as those on the recommended test equipment list.

Contact your local ANRITSU service center (refer to Table 1-5 on page 1-18) if you need clarification of any equipment or procedural reference.

3-3 TEST RECORDS

A blank copy of a sample performance verification test record for each 690XXA/691XXA model is provided in Appendix A. Each test record contains the model-specific variables called for by the test procedures. It also provides a means for maintaining an accurate and complete record of instrument performance. We recommend that you copy these pages and use them to record the results of your initial testing of the instrument. These initial test results can later be used as benchmark values for future tests of the same instrument.

3-4 CONNECTOR AND KEY LABEL NOTATION

The test procedures include many references to equipment interconnections and control settings. For all 690XXA/691XXA references, specific labels are used to denote the appropriate menu key, data entry key, data entry control, or connector (such as CW/SWEEP SELECT or RF OUTPUT). Most references to supporting test equipment use general labels for commonly used controls and connections (such as Span or RF Input). In some cases, a specific label is used that is a particular feature of the test equipment listed in Table 3-1.

Table 3-1. *Recommended Test Equipment for Performance Verification Tests (1 of 2)*

INSTRUMENT	CRITCAL SPECIFICATION	RECOMMENDED MANUFACTURER/MODEL	TEST NUMBER
Spectrum Analyzer, with External Mixers and Diplexer Assy	*Frequency Resolution:* 0.01 to 65 GHz *Resolution Bandwidth:* 10 Hz	Tektronix, Model 2794, with External Mixers: WM780K (18 to 26.5 GHz) WM780A (26.5 to 40 GHz) WM780U (40 to 60 GHz) WM780E (60 to 90 GHz) and Diplexer Assy: 015-385-00	3-8, 3-9
Spectrum Analyzer	*Frequency Range:* 20 Hz to 40 MHz *Resolution Bandwidth:* 3 Hz	Hewlett-Packard, Model 3585B	3-10
Frequency Counter with Cable Kit and External Mixer	*Frequency Range:* 0.01 to 65 GHz *Input Impedance:* 50Ω *Resolution:* 1 Hz *Other:* External Time Base Input	EIP Microwave, Inc. Models 538B, 548B, or 578B, with Cable Kit: Option 590 and External Mixer: Option 91 (26.5 to 40 GHz) Option 92 (40 to 60 GHz) Option 93 (60 to 90 GHz)	3-7
Power Meter, with Power Sensor	*Power Range:* –30 to +20 dBm (1μW to 100mW)	Hewlett-Packard Model 437B, with Power Sensor: HP 8487A (0.01 to 50 GHz)	3-11
Power Meter with Power Sensor	*Power Range:* –30 to +20 dBm (1μW to 100mW)	ANRITSU ML4803A, with Power Sensor: MP716A4 (50 to 75 GHz)	3-11
Frequency Reference	*Frequency:* 10 MHz *Accuracy:* 5 x 10^{-12} parts/day	Absolute Time Corp., Model 300	3-6
Oscilloscope	*Bandwidth:* DC to 150 MHz *Vertical Sensitivity:* 2mV/division *Horizontal Sensitivity:* 50 ns/division	Tektronix, Inc. Model TAS485	3-6, 3-11
Mixer	*Frequency Range:* 1 to 26 GHz	Macom Micro Electronics Div. Model DMS1-26A	3-10
Adapter	K (male) to 2.4 mm (female) Adapts the Power Sensor, HP 8487A, to the 690XXA/691XXA RF OUTPUT connector (≤40 GHz models)	Hewlett-Packard Part Number: HP 11904D	3-11
Adapter	Adapts the MP716A4 Power Sensor to the ML4803A Power Meter	ANRITSU MA4002B	3-11
Adapter	WR15 to V (male) Adapts the MP716A4 Power Sensor to the 690XXA/691XXA RF OUTPUT connector (>40 GHz)	ANRITSU, Model 35WR15V	3-11
Attenuator	*Frequency Range:* DC to 40 GHz *Max Input Power:* .+17 dBm *Attenuation:* 10 dB	ANRITSU, Model 41KC-10	3-9, 3-10

Table 3-1. *Recommended Test Equipment for Performance Verification Tests (2 of 2)*

INSTRUMENT	CRITCAL SPECIFICATION	RECOMMENDED MANUFACTURER/MODEL	TEST NUMBER
Attenuator	*Frequency Range:* DC to 40 GHz *Max Input Power:* >+17 dBm *Attenuation:* 20 dB	ANRITSU, Model 41KC-20	3-9
Attenuator	*Frequency Range:* DC to 60 GHz *Max Input Power:* .+17 dBm *Attenuation:* 10 dB	ANRITSU, Model 41V-10	3-9, 3-10
Attenuator	*Frequency Range:* DC to 60 GHz *Max Input Power:* >+17 dBm *Attenuation:* 20 dB	ANRITSU, Model 41V-20	3-9
Tee	*Connectors:* 50Ω BNC	Any common source	3-10
Cables	*Connectors:* 50Ω BNC	Any common source	All tests

3-5 690XXA/691XXA POWER LEVELS

Table 3-2 is a listing of the Series 690XXA and 691XXA Synthesized CW/Sweep Generator models and their maximum leveled ouput power levels. Certain test procedures will refer you to this table for the maximum leveled output power level setting of the instrument model being tested.

Table 3-2. *690XXA/691XXA Maximum Leveled Output Power (1 of 2)*

69XXXA Model	Frequency (GHz)	Max Leveled Output Power	Max Leveled Output Power w/Step Attenuator
69X37A	2.0 – 20.0 GHz	+13.0 dBm	+11.0 dBm
69X45A	0.5 – 20.0 GHz	+13.0 dBm	+11.0 dBm
69X47A	0.01 – 20.0 GHz	+13.0 dBm	+11.0 dBm
69X53A	2.0 – 20.0 GHz 20.0 – 26.5 GHz	+9.0 dBm +6.0 dBm	+7.0 dBm +3.5 dBm
69X55A	0.5 – 2.2 GHz 2.2 – 20.0 GHz 20.0 – 26.5 GHz	+13.0 dBm +9.0 dBm +6.0 dBm	+11.0 dBm +7.0 dBm +3.5 dBm
69X59A	0.01 – 2.0 GHz 2.0 – 20.0 GHz 20.0 – 26.5 GHz	+13.0 dBm +9.0 dBm +6.0 dBm	+11.0 dBm +7.0 dBm +3.5 dBm
69X63A	2.0 – 20.0 GHz 20.0 – 40.0 GHz	+9.0 dBm +6.0 dBm	+7.0 dBm +3.0 dBm
69X65A	0.5 – 2.2 GHz 2.2 – 20.0 GHz 20.0 – 40.0 GHz	+13.0 dBm +9.0 dBm +6.0 dBm	+11.0 dBm +7.0 dBm +3.0 dBm
69X69A	0.01 – 2.0 GHz 2.0 – 20.0 GHz 20.0 – 40.0 GHz	+13.0 dBm +9.0 dBm +6.0 dBm	+11.0 dBm +7.0 dBm +3.0 dBm
69X75A	0.5 – 2.2 GHz 2.2 – 20.0 GHz 20.0 – 40.0 GHz 40.0 – 50.0 GHz	+11.0 dBm +10.0 dBm +2.5 dBm +2.5 dBm	+10.0 dBm +8.5 dBm 0.0 dBm –1.0 dBm
69X77A	0.01 – 2.0 GHz 2.0 – 20.0 GHz 20.0 – 40.0 GHz 40.0 – 50.0 GHz	+12.0 dBm +10.0 dBm +2.5 dBm +2.5 dBm	+10.0 dBm +8.5 dBm 0.0 dBm –1.0 dBm
69X85A	0.5 – 2.2 GHz 2.2 – 20.0 GHz 20.0 – 40.0 GHz 40.0 – 50.0 GHz 50.0 – 60.0 GHz	+11.0 dBm +10.0 dBm +2.5 dBm +2.0 dBm +2.0 dBm	+10.0 dBm +8.5 dBm 0.0 dBm –1.5 dBm –2.0 dBm
69X87A	0.01 – 2.0 GHz 2.0 – 20.0 GHz 20.0 – 40.0 GHz 40.0 – 50.0 GHz 50.0 – 60.0 GHz	+12.0 dBm +10.0 dBm +2.5 dBm +2.0 dBm +2.0 dBm	+10.0 dBm +8.5 dBm 0.0 dBm –1.5 dBm –2.0 dBm

Table 3-2. *690XXA/691XXA Maximum Leveled Output Power (2 of 2)*

69XXXA Model	Frequency (GHz)	Max Leveled Output Power	Max Leveled Output Power w/Step Attenuator
69X95A	0.5 – 2.2 GHz 2.2 – 20.0 GHz 20.0 – 40.0 GHz 40.0 – 50.0 GHz 50.0 – 65.0 GHz	+11.0 dBm +10.0 dBm +2.5 dBm 0.0 dBm –2.0 dBm	Not Available
69X97A	0.01 – 2.0 GHz 2.0 – 20.0 GHz 20.0 – 40.0 GHz 40.0 – 50.0 GHz 50.0 – 65.0 GHz	+12.0 dBm +10.0 dBm +2.5 dBm 0.0 dBm –2.0 dBm	Not Available
With Option 15A (High Power) Installed			
69X37A	2.0 – 20.0 GHz	+17.0 dBm	+15.0 dBm
69X45A	0.5 – 2.2 GHz 2.0 – 20.0 GHz	+13.0 dBm +17.0 dBm	+11.0 dBm +15.0 dBm
69X47A	0.01 – 2.0 GHz 2.0 – 20.0 GHz	+13.0 dBm +17.0 dBm	+11.0 dBm +15.0 dBm
69X53A	2.0 – 20.0 GHz 20.0 – 26.5 GHz	+13.0 dBm +10.0 dBm	+11.0 dBm +7.5 dBm
69X55A	0.5 – 2.2 GHz 2.2 – 20.0 GHz 20.0 – 26.5 GHz	+13.0 dBm +13.0 dBm +10.0 dBm	+11.0 dBm +11.0 dBm +7.5 dBm
69X59A	0.01 – 2.0 GHz 2.0 – 20.0 GHz 20.0 – 26.5 GHz	+13.0 dBm +13.0 dBm +10.0 dBm	+11.0 dBm +11.0 dBm +7.5 dBm
69X63A	2.0 – 20.0 GHz 20.0 – 40.0 GHz	+13.0 dBm +6.0 dBm	+11.0 dBm +3.0 dBm
69X65A	0.5 – 2.2 GHz 2.2 – 20.0 GHz 20.0 – 40.0 GHz	+13.0 dBm +13.0 dBm +6.0 dBm	+11.0 dBm +11.0 dBm +3.0 dBm
69X69A	0.01 – 2.0 GHz 2.0 – 20.0 GHz 20.0 – 40.0 GHz	+13.0 dBm +13.0 dBm +6.0 dBm	+11.0 dBm +11.0 dBm +3.0 dBm
69X75A	0.5 – 50.0 GHz	Standard	Standard
69X77A	0.01 – 50.0 GHz	Standard	Standard
69X85A	0.5 – 60.0 GHz	Standard	Standard
69X87A	0.01 – 60.0 GHz	Standard	Standard
69X95A	0.5 – 65.0 GHz	Standard	Not Available
69X97A	0.01 – 65.0 GHz	Standard	Not Available

3-6 INTERNAL TIME BASE AGING RATE TEST (Optional)

The following test can be used to verify that the 690XXA/691XXA 10 MHz time base is within its aging specification. The instrument derives its frequency accuracy from an internal 100 MHz crystal oscillator standard. (With Option 16 installed, frequency accuracy is derived from an internal high-stability 10 MHz crystal oscillator.) An inherent characteristic of crystal oscillators is the effect of crystal *aging* within the first few days to weeks of operation. Typically, the crystal oscillator's frequency increases slightly at first, then settles to a relatively constant value for the rest of its life. The 690XXA/691XXA reference oscillator aging is specified as $<2x10^{-8}$ parts per day ($<5x10^{-10}$ with Option 16).

NOTE

Do not confuse crystal aging with other short term frequency instabilities; i.e., noise and temperature. The internal time base of the instrument may not achieve its specified aging rate before the specified warm-up time of 7 to 30 days has elasped; therefore, this performance test is optional.

For greatest absolute frequency accuracy, allow the 690XXA/691XXA to warm up until its RF output frequency has stabilized (usually 7 to 30 days). Once stabilized, the change in reference oscillator frequency should remain within the aging rate if; (1) the time base oven is not allowed to cool, (2) the instrument orientation with respect to the earth's magnetic field is maintained, (3) the instrument does not sustain any mechanical shock, and (4) ambient temperature is held constant. This test should be performed upon receipt of the instrument and again after a period of several days to weeks to fully qualify the aging rate.

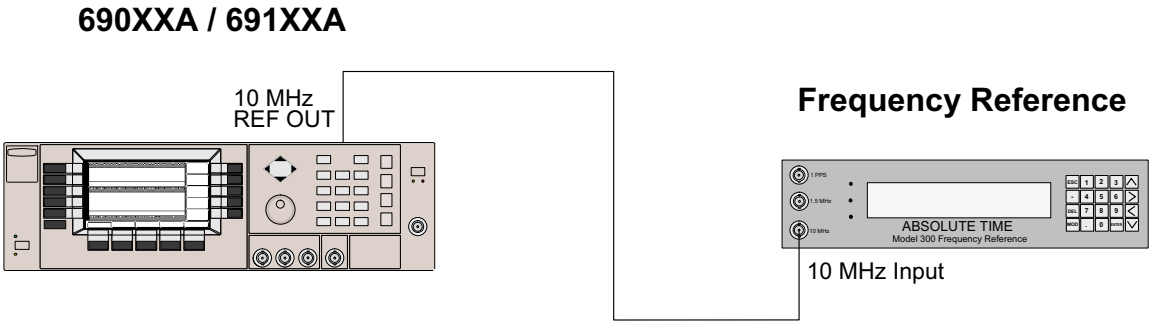

Figure 3-1. *Equipment Setup for Internal Time Base Aging Rate Test*

Test Setup Connect the 690XXA/691XXA rear panel 10 MHz REF OUT to the Frequency Reference front panel input connector labeled 10 MHz when directed to do so during the test procedure.

Test Procedure

The frequency error is measured at the start and finish of the test time period of 24 hours. The aging rate is the difference between the two error readings.

1. Set up the Frequency Reference as follows:
   a. Press the **ESC** key until the MAIN MENU is displayed.
   b. At the MAIN MENU display, press **1** to select CONFIGURATION.
   c. At the CONFIGURATION MENU display, press **8** to select MEAS.
   d. Press the **MOD** key and use the Up/Down Arrow keys to get back to the menu display: MEASUREMENT = FREQ.
   e. Press the **ENTER** key.
   f. Press the **ESC** key until the MAIN MENU is displayed.
   g. At the MAIN MENU display, press **3** to select the REVIEW MENU.
   h. At the REVIEW MENU display, press **8** to select TFM.
2. Connect the 690XXA/691XXA rear panel 10 MHz REF OUT signal to the Frequency Reference front panel 10 MHz input.
3. Wait approximately 90 minutes (default setting) until the FMFOM on the Frequency Reference display decreases from 9 to 1. (The default setting is recommended to achieve optimum measurements.)

   The frequency errror in the signal under test is displayed in ps/s (Picosecond/Second). For example, an error of –644681 ps/s is -644681×10^{-12} or -6.44681×10^{-7} away from the 10 MHz internal reference of the Frequency Reference.

   The frequency error display is continuously updated as a running 5000-second average. the averaging smooths out the short-term instability of the oscillator.

4. Record the frequency error value, displayed on the Frequency Reference, on the Test Record.

5. Wait for 24 hours, then record the current frequency error value on the Test Record.

6. The aging rate is the difference between the two frequency error values.

7. Record the computed result on the Test Record. To meet the specification, the computed aging rate must be $<2x10^{-8}$ per day ($<5x10^{-10}$ per day with Option 16).

3-7 FREQUENCY SYNTHESIS TESTS

The following tests can be used to verify correct operation of the frequency synthesis circuits. Frequency synthesis testing is divided into two parts—coarse loop/YIG loop tests and fine loop tests.

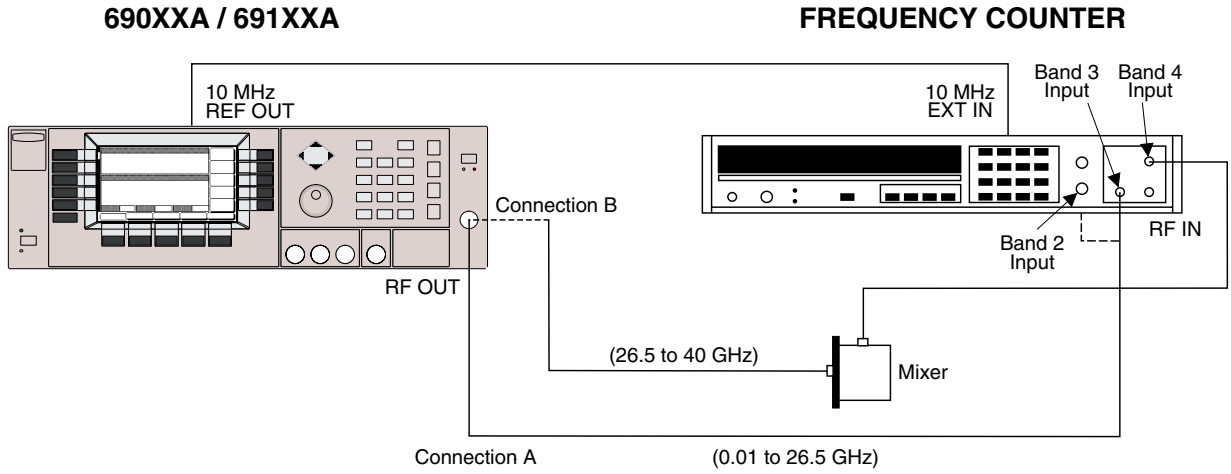

Figure 3-2. *Equipment Setup for Frequency Synthesis Tests*

Test Setup

Connect the equipment, shown in Figure 3-2, as follows:

1. Connect the 690XXA/691XXA rear panel 10 MHz REF OUT to the Frequency Counter 10 MHz External Reference input. If the Frequency Counter has an INT/EXT toggle switch, ensure the switch is set to EXT.

2. Connect the 690XXA/691XXA RF OUTPUT to the Frequency Counter RF Input as follows:
   a. For measuring frequencies of 0.01 to 1.0 GHz, connect to the Band 2 input (Connection A).
   b. For measuring frequencies of 1.0 to 26.5 GHz, connect to the Band 3 input (Connection A).
   c. For measuring frequencies of 26.5 to 40.0 GHz, connect to the Band 4 input via the Option 91 waveguide mixer (Connection B).
   d. For measuring frequencies of 40.0 to 60.0 GHz, connect to the Band 4 input via the Option 92 waveguide mixer (Connection B).
   e. For measuring frequencies of 60.0 to 65.0 GHz, connect to the Band 4 input via the Option 93 waveguide mixer (Connection B).

Coarse Loop/ YIG Loop Test Procedure

The following procedure tests both the coarse loop and YIG loop by stepping the instrument through its full frequency range in 1 GHz steps and measuring the RF output at each step.

1. Set up the 690XXA/691XXA as follows:
   a. Reset the instrument by pressing **SYSTEM**, then Reset. Upon reset, the CW Menu is displayed.
   b. Press Edit F1 to open the current frequency parameter for editing.
   c. Set F1 to the first test frequency indicated on the Test Record for the model being tested.

2. Record the Frequency Counter reading on the Test Record. The Frequency Counter reading must be within ±100 Hz of the displayed 690XXA/691XXA frequency to accurately complete this test.

   NOTE
   The Frequency Counter reading is typically within ±1 Hz because the instruments use a common time base. Differences of a few Hertz can be caused by noise or counter limitations. Differences of ≥±100 Hz indicate a frequency synthesis problem.

3. On the 690XXA/691XXA, use the cursor control key (diamond-shaped key) to increment F1 to the next test frequency on the Test Record. Record the Frequency Counter reading on the Test Record.

4. Repeat step 3 until all frequencies listed on the Test Record have been recorded.

Fine Loop Test Procedure

The following procedure tests the fine loop by stepping the instrument through ten 1 kHz steps (ten 100 Hz steps for instruments with Option 11) and measuring the RF output at each step.

1. Set up the 690XXA/691XXA as follows:
   a. Reset the instrument by pressing **SYSTEM**, then Reset. Upon reset, the CW Menu is displayed.
   b. Press Edit F1 to open the current frequency parameter for editing.
   c. Set F1 to the first test frequency indicated on the Test Record.
2. Record the Frequency Counter reading on the Test Record. The Frequency Counter reading must be within ±100 Hz of the displayed 690XXA/691XXA frequency (±10 Hz for instruments with Option 11) to accurately complete this test.
3. On the 690XXA/691XXA, use the cursor control key (diamond-shaped key) to increment F1 to the next test frequency on the Test Record. Record the Frequency Counter reading on the Test Record.
4. Repeat step 3 until all frequencies listed on the Test Record have been recorded.

3-8 SPURIOUS SIGNALS TEST: RF OUTPUT SIGNALS ≤2 GHz (≤2.2 GHz for 69XX5A MODELS)

The following test can be used to verify that the CW/sweep generator meets it spurious signal specifications for RF output signals from 0.01 to 2 GHz (0.5 to 2.2 GHz for 69XX5A models). This test is applicable only to instruments which cover the frequency range 10 MHz to 2 GHz (500 MHz to 2.2 GHz for 69XX5A models). The 0.01 to 2 GHz test procedure begins on this page; the 0.5 to 2.2 GHz test procedure begins on page 3-17.

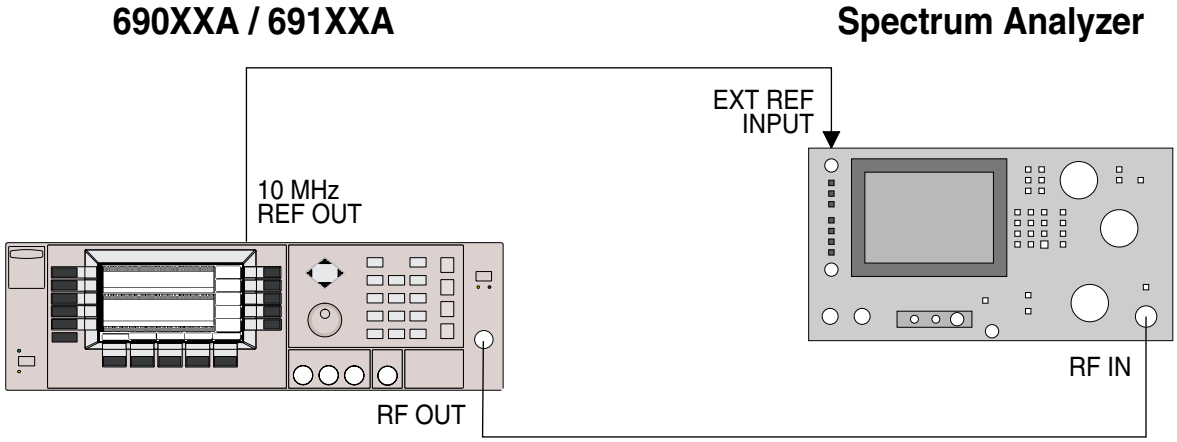

Figure 3-3. *Equipment Setup for Spurious Signals Test: RF Output Signals ≤2 GHz (≤2.2 GHz for 69XX5As)*

Test Setup

Connect the equipment, shown in Figure 3-3, as follows:

1. Connect the 690XXA/691XXA rear panel 10 MHz REF OUT to the Spectrum Analyzer External Reference Input.
2. Connect the 690XXA/691XXA RF OUTPUT to the Spectrum Analyzer RF Input.

0.01 - 2 GHz Test Procedure

The following procedure lets you measure the worst case spurious signals (harmonic and non-harmonic) of the 0.01 to 2 GHz RF output to verify that they meet specifications.

1. Set up the Spectrum Analyzer as follows:
   a. Span: 10 MHz/div
   b. CF: 50 MHz
   c. RBW: 1 MHz
   d. Sweep Time/Div: Auto (to resolve signal peaks clearly)

Table 3-3. *Spurious Signals Specifications*

Harmonic and Harmonic Related:	
500 MHz to ≤2.2 GHz (69XX5A):	<–50 dBc
10 MHz to ≤50 MHz:	<–30 dBc
>50 MHz to ≤2 GHz:	<–40 dBc
>2 GHz (2.2 GHz for 69XX5A) to ≤20 GHz:	<–60 dBc
>20 GHz to ≤40 GHz:	<–40 dBc
Harmonic and Harmonic Related (Models having a high-end frequency of >40 GHz and units with Option 15A at maximum specified leveled output power):	
500 MHz to ≤2.2 GHz (69XX5A):	<–50 dBc
10 MHz to ≤50 MHz:	<–30 dBc
>50 Mhz to ≤2 GHz:	<–40 dBc
>2 GHz (2.2 GHz for 69XX5A) to ≤20 GHz:	<–50 dBc
>20 GHz to ≤40 GHz:	<–40 dBc
50 GHz units: >40 GHz to ≤50 GHz:	<–40 dBc
60 GHz units: >40 GHz to ≤60 GHz:	<-30 dBc
65 GHz units: >40 GHz to ≤45 GHz:	<–25 dBc
>45 GHz to ≤65 GHz:	<-30 dBc
Non-Harmonics:	
500 MHz to ≤2.2 GHz (69XX5A):	<–50 dBc
10 MHz to ≤2 GHz:	<–40 dBc
>2 GHz (2.2 GHz for 69XX5A) to ≤65 GHz:	<–60 dBc

2. Set up the 690XXA/691XXA as follows:
   a. Reset the instrument by pressing **SYSTEM**, then Reset. Upon reset the CW Menu is displayed.
   b. Press Edit L1 to open the current power level parameter for editing.
   c. Set L1 to the lesser of +10 dBm or the maximum leveled power level for the instrument being tested (refer to Table 3-2, page 3-6).
   d. Press Edit F1 to open the current frequency parameter for editing.
   e. Set F1 to 10 MHz.
3. On the Spectrum Analyzer, measure the worst case harmonic and non-harmonic signals for the 10 MHz carrier. Record their presence by entering the levels on the Test Record. Refer to Table 3-3 for the specified level limits.

   NOTE
   Harmonics appear at multiples of the CW frequency and diminish quickly as the CW frequency gets greater than 1 GHz.

4. Repeat step 3 with F1 set first to 20 MHz, then set to 30 MHz. Measure the worst case harmonics and non-harmonics for each carrier frequency and record their presence by entering their levels on the Test Record.
5. Change the Spectrum Analyzer setup as follows:
   a. Span: 100 MHz/div
   b. CF: 500 MHz
6. Repeat step 3 with F1 set to 40 MHz. Measure the worst case harmonic and non-harmonic signals for the 40 MHz carrier and record their presence by entering their levels on the Test Record.
7. Change the Spectrum Analyzer setup as follows:
   a. Span: 200 MHz/div (or maximum span width)
   b. CF: 1 GHz (N/A if at maximum span width)
8. Repeat step 3 with F1 set to 350 MHz. Measure the worst case harmonic and non-harmonic signals for the 350 MHz carrier and record their

presence by entering their levels on the Test Record.

9. Set F1 to 1.6 GHz. Measure the worst case non-harmonic signal for the 1.6 GHz carrier and record its presence by entering its level on the Test Record.

10. Change the Spectrum Analyzer setup as follows:
    a. Span: 10 MHz/div
    b. CF: 1.6 GHz
    c. RBW: 1 MHz

11. Adjust the Spectrum Analyzer Reference Level control to place the signal at the top of the screen graticule.

12. Change the Spectrum Analyzer CF first to 3.2 GHz, then to 4.8 GHz. Compare the harmonic levels with the signal level at 1.6 GHz. Measure the harmonic levels and record them on the Test Record.

0.5 - 2.2 GHz Test Procedure

The following procedure lets you measure the 0.5 to 2.2 GHz RF output harmonic levels to verify that they meet specifications.

1. Set up the 690X5A/691X5A as follows:
   a. Reset the instrument by pressing **SYSTEM**, then Reset. Upon reset the CW Menu is displayed.
   b. Press Edit L1 to open the current power level parameter for editing.
   c. Set L1 to the lesser of +10 dBm or the maximum leveled power level for the instrument being tested (refer to Table 3-2, page 3-6).
   d. Press Edit F1 to open the current frequency parameter for editing.
   e. Set F1 to the frequency indicated on the Test Record.

2. Set up the Spectrum Analyzer as follows:
   a. Span: 5 kHz/div
   b. CF: Set to the 690X5A/691X5A frequency value.
   c. RBW: 1 kHz
   d. Video Filter Wide: On

3. Adjust the Spectrum Analyzer Peaking control for maximum signal level, then adjust the Reference Level Control to place the signal at the top of the screen graticule.

4. Change the Spectrum Analyzer CF to each of the harmonic frequencies listed on the Test Record and record the signal levels on the Test Record. Refer to Table 3-3 (page 3-15) for the specified harmonic signal level limits.

5. Repeat steps 1 through 4 for each of the 690X5A/691X5A CW carrier and harmonic frequencies listed on the Test Record. Record the harmonic signal levels on the Test Record.

3-9 HARMONIC TEST: RF OUTPUT SIGNALS FROM 2 TO 20 GHz

The following test can be used to verify that the 690XXA/691XXA meets its harmonic specifications for RF output signals from 2 to 20 GHz (2.2 to 20 GHz for 69XX5A Models). Test record entries are supplied for harmonics up to a frequency limit of 40 GHz. Additional harmonic checks may be made at any frequency of interest up to the RF output frequency limit of the 690XXA/691XXA model being tested. These additional harmonic checks can be accomplished through the use of waveguide mixers to extend the frequency range of the spectrum analyzer.

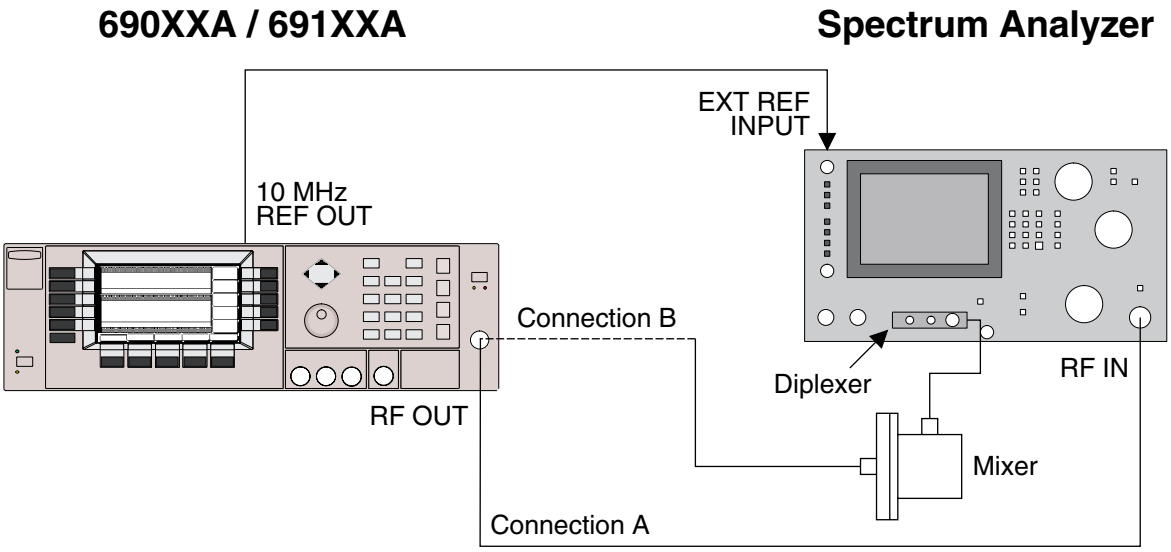

Figure 3-4. *Equipment Setup for Harmonic Test: RF Output Signals from 2 to 20 GHz (2.2 to 20 GHz for 69XX5As)*

Test Setup

Connect the equipment, shown in Figure 3-4, as follows:

1. Connect the 690XXA/691XXA rear panel 10 MHz REF OUT to the Spectrum Analyzer External Reference Input.
2. Connect the diplexer and appropriate external waveguide mixer to the Spectrum Analyzer.
3. Connect the 690XXA/691XXA RF OUTPUT to the Spectrum Analyzer as shown in Connection A (690XXA/691XXA RF OUTPUT to Spectrum Analyzer RF IN).

2 - 10 GHz Test Procedure

The following procedure lets you measure the 2 to 10 GHz (2.2 to 10 GHz for 69XX5As) RF output harmonic levels to verify that they meet specifications.

1. Set up the 690XXA/691XXA as follows:
   a. Reset the instrument by pressing **SYSTEM**, then Reset. Upon reset the CW Menu is displayed.
   b. Press Edit L1 to open the current power level parameter for editing.
   c. Set L1 to the lesser of +10 dBm or the maximum leveled power level for the instrument being tested (refer to Table 3-2, page 3-6).
   d. Press Edit F1 to open the current frequency parameter for editing.
   e. Set F1 to the frequency indicated on the Test Record.

2. Set up the Spectrum Analyzer as follows:
   a. Span: 5 kHz/div
   b. CF: Set to the 690XXA/691XXA frequency value.
   c. RBW: 1 kHz
   d. Video Filter Wide: On

3. Adjust the Spectrum Analyzer Peaking control for maximum signal level, then adjust the Reference Level Control to place the signal at the top of the screen graticule.

4. Change the Spectrum Analyzer CF to each of the harmonic frequencies listed on the Test Record and record the signal levels. Refer to Table 3-4 for the specified harmonic signal level limits.

5. Repeat steps 1 through 4 for each of the 690XXA/691XXA CW carrier and harmonic frequencies listed on the Test Record. Record the harmonic signal levels on the Test Record.

Table 3-4. *Spurious Signals Specifications*

Harmonic and Harmonic Related:	
500 MHz to ≤2.2 GHz (69XX5A):	<–50 dBc
10 MHz to ≤50 MHz:	<–30 dBc
>50 MHz to ≤2 GHz:	<–40 dBc
>2 GHz (2.2 GHz for 69XX5A) to ≤20 GHz:	<–60 dBc
>20 GHz to ≤40 GHz:	<–40 dBc
Harmonic and Harmonic Related (Models having a high-end frequency of >40 GHz and units with Option 15A at maximum specified leveled output power):	
500 MHz to ≤2.2 GHz (69XX5A):	<–50 dBc
10 MHz to ≤50 MHz:	<–30 dBc
>50 MHz to ≤2 GHz:	<–40 dBc
>2 GHz (2.2 GHz for 69XX5A) to ≤20 GHz:	<–50 dBc
>20 GHz to ≤40 GHz:	<–40 dBc
50 GHz units: >40 GHz to ≤50 GHz:	<–40 dBc
60 GHz units: >40 GHz to ≤60 GHz:	<–30 dBc
65 GHz units: >40 GHz to ≤45 GHz:	<–25 dBc
>45 GHz to ≤65 GHz:	<–30 dBc
Non-Harmonics:	
500 MHz to ≤2.2 GHz (69XX5A):	<–50 dBc
10 MHz to ≤2 GHz:	<–40 dBc
>2 GHz (2.2 GHz for 69XX5A) to ≤65 GHz:	<–60 dBc

11 - 20 GHz Test Procedure

The following procedure lets you measure the 11 to 20 GHz RF output harmonic levels to verify that they meet specifications.

NOTE

Because an external mixer is required for these measurements, the RF output flatness of the 690XXA/691XXA instrument is used to correct for; (1) variations caused by switching from the fundamental input to the external mixer input of the Spectrum Analyzer, and (2) the flatness of the mixer.

1. Set up the 690XXA/691XXA as follows:
   a. Reset the instrument by pressing **SYSTEM**, then Reset. Upon reset the CW Menu is displayed.
   b. Press Edit F1 to open the current frequency parameter for editing.
   c. Set F1 to the frequency indicated on the Test Record.
   d. Press Edit L1 to open the current power level parameter for editing.
   e. Set L1 to –30 dBm output power.

NOTE

If the 690XXA/691XXA is not fitted with Option 2, install a 30 dB attenuator (ANRITSU 41KC-20 and 41KC-10 for ≤40 GHz models; 41V-20 and 41V-10 for >40 GHz models) and set L1 to 0.0 dBm output power.

2. Set up the Spectrum Analyzer as follows:
   a. Span: 5 kHz/div
   b. CF: Set to the 690XXA/691XXA frequency value.
   c. RBW: 1 kHz
   d. Video Filter Wide: On
3. Adjust the Spectrum Analyzer Peaking control for maximum signal, then adjust the Reference Level control to place the signal at the top of the screen graticule. It may be necessary to also adjust the 690XXA/691XXA output power level

slightly to accomplish this; however, *do not exceed –20 dBm output power.*

4. Remove Connection A and connect the 690XXA/691XXA RF OUTPUT to the waveguide mixer input of the Spectrum Analyzer as shown in Connection B.

5. On the 690XXA/691XXA, remove 30 dB of attenuation from the RF output. Do this by either increasing the output power level by 30 dB or by removing the 30 dB attenuator installed in step 1.e.

6. Change the Spectrum Analyzer CF to the harmonic frequency listed on the Test Record. Verify that the signal displayed on the Spectrum Analyzer is ≥30 dB below the top of the screen graticule.

NOTE

The <–30 dB signal level plus the 30 dB attenuation provided by the waveguide mixer equals a harmonic frequency signal level of <–60 dBc (specification).

7. Record the harmonic signal level on the Test Record.

8. Repeat steps 1 through 7 for each of the 690XXA/691XXA CW carrier and harmonic frequencies listed on the Test Record. Record the harmonic signal levels on the Test Record.

3-10 SINGLE SIDEBAND PHASE NOISE TEST

The following test can be used to verify that the 690XXA/691XXA meets its single sideband phase noise specifications. For this test, a second 690XXA/691XXA is required. This additional instrument acts as a local oscillator (LO). The CW RF output of the 690XXA/691XXA under test (DUT) is mixed with the CW RF output from the 690XXA/691XXA LO which is offset by 1 MHz. Single sideband phase noise is measured at offsets of 100 Hz, 1 kHz, 10 kHz, and 100 kHz away from the resultant 1 MHz IF.

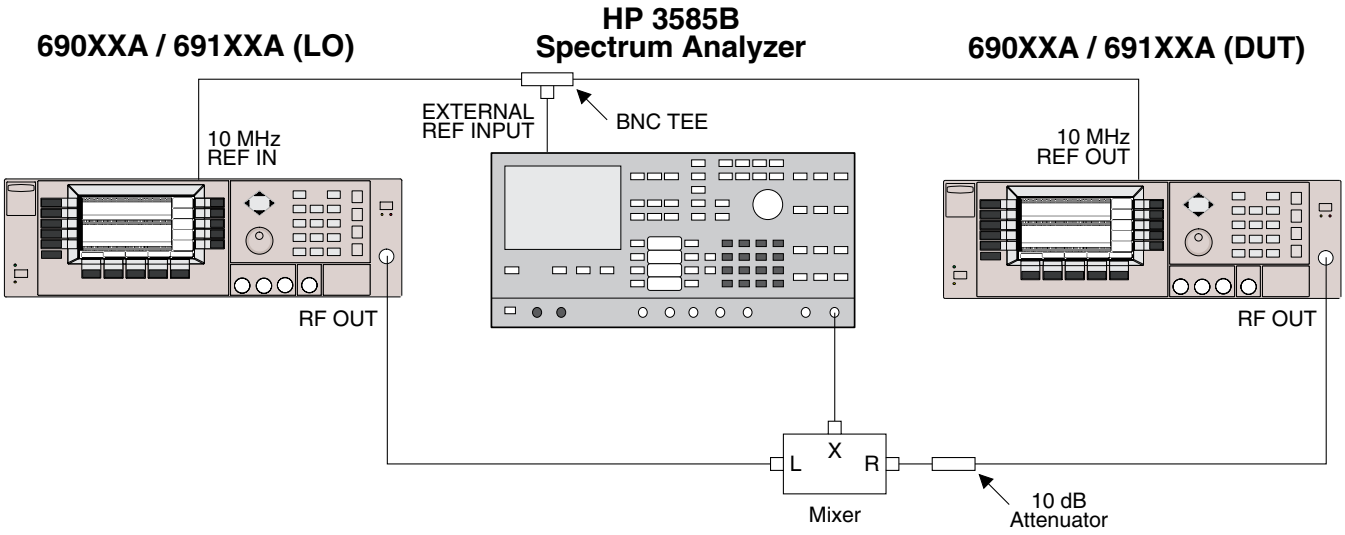

Figure 3-5. *Equipment Setup for Single Sideband Phase Noise Test*

Test Setup

Connect the equipment, shown in Figure 3-5, as follows:

1. Connect the 690XXA/691XXA DUT rear panel 10 MHz REF OUT to the BNC tee. Connect one leg of the tee to the 690XXA/691XXA LO rear panel 10 MHz REF IN. Connect the other leg of the tee to the Spectrum Analyzer External Reference Input.

2. Connect the 690XXA/691XXA DUT RF OUTPUT to the Mixer's R input via a 10 dB attenuator.

3. Connect the 690XXA/691XXA LO RF OUTPUT to the Mixer's L input.

4. Connect the Mixer's X output to the Spectrum Analyzer 50Ω input.

Test Procedure

The following procedure lets you measure the RF output single sideband phase noise levels to verify that they meet specifications.

NOTE

The following technique is a measurement of phase noise and AM noise. To avoid erroneous results, on the 690XXA/691XXA DUT set L1 for maximum leveled output power and select External Detector leveling. This will prevent any AM noise from degrading the phase noise measurements.

1. Set up the 690XXA/691XXA DUT as follows:
   a. Reset the instrument by pressing **SYSTEM**, then Reset. Upon reset the CW Menu is displayed.
   b. Press Edit F1 to open the current frequency parameter for editing.
   c. Set F1 to the frequency indicated on the Test Record.
   d. Press Edit L1 to open the current power level parameter for editing.
   e. Set L1 to the maximum leveled power level for the instrument being tested (refer to Table 3-2, page 3-6).

2. Set up the 690XXA/691XXA LO as follows:
   a. Reset the instrument by pressing **SYSTEM**, then Reset. Upon reset the CW Menu is displayed.
   b. Press Edit F1 to open the current frequency parameter for editing.
   c. Set F1 to a frequency that is 1 MHz lower than the 690XXA/691XXA DUT frequency set in step 1.c.
   d. Press Edit L1 to open the current power level parameter for editing.
   e. Set L1 to the maximum leveled power level for the instrument model (refer to Table 3-2).

Table 3-7. *Single Sideband Phase Noise Test Specification*

CW Carrier Frequency	Offset From Carrier	Test Specification*
0.6 GHz	100 Hz	<–77 dBc
	1 kHz	<–95 dBc
	10 kHz	<–97 dBc
	100 kHz	<–99 dBc
0.6 GHz (69XX5A)	100 Hz	<–89 dBc
	1 kHz	<–109 dBc
	10 kHz	<–109 dBc
	100 kHz	<–114 dBc
2.0 GHz	100 Hz	<–77 dBc
	1 kHz	<–97 dBc
	10 kHz	<–97 dBc
	100 kHz	<–102 dBc
2.0 GHz (69XX5A)	100 Hz	<–83 dBc
	1 kHz	<–103 dBc
	10 kHz	<–103 dBc
	100 kHz	<–108 dBc
6.0 GHz	100 Hz	<–75 dBc
	1 kHz	<–97 dBc
	10 kHz	<–97 dBc
	100 kHz	<–102 dBc
10.0 GHz	100 Hz	<–71 dBc
	1 kHz	<–95 dBc
	10 kHz	<–97 dBc
	100 kHz	<–102 dBc
20.0 GHz	100 Hz	<–63 dBc
	1 kHz	<–92 dBc
	10 kHz	<–97 dBc
	100 kHz	<–99 dBc
26.5 GHz	100 Hz	<–60 dBc
	1 kHz	<–88 dBc
	10 kHz	<–91 dBc
	100 kHz	<–93 dBc

* 3 dB difference from 690XXA/691XXA single sideband phase noise specifications to account for LO phase noise.

NOTE

If the 690XXA/691XXA LO output is less than 10 dBm, the Mixer's local oscillator port will not be saturated and the resulting measurements may be in error.

3. Set up the Spectrum Analyzer as follows:
   a. Center Frequency: 1 MHz
   b. Frequency Span: 300 Hz
   c. RBW: 3 Hz
   d. Position the Marker to the peak of the signal.
   e. Select OFFSET, ENTER OFFSET, and MKRCF.
   f. Adjust the marker for a 100 Hz offset.
   g. Select NOISE LVL.
4. Measure the phase noise level 100 Hz offset from the carrier frequency. Record the level on the Test Record.
5. On the Spectrum Analyzer:
   a. Deselect NOISE LVL.
   b. Set Frequency Span to 20 kHz.
   c. Set RBW to 100 Hz.
   d. Adjust the Marker for a 1 kHz offset.
   e. Select NOISE LVL.
6. Measure the phase noise level 1 kHz offset from the carrier frequency. Record the level on the Test Record.
7. On the Spectrum Analyzer:
   a. Deselect NOISE LVL.
   b. Set Frequency Span to 100 kHz.
   c. Adjust the Marker for a 10 kHz offset.
   d. Select NOISE LVL.
8. Measure the phase noise level 10 kHz offset from the carrier frequency. Record the level on the Test Record.

9. On the Spectrum Analyzer:
   a. Deselect NOISE LVL.
   b. Set Frequency Span to 300 kHz.
   c. Adjust the Marker for a 100 kHz offset.
   d. Select NOISE LVL.
10. Measure the phase noise level 100 kHz offset from the carrier frequency. Record the level on the Test Record.
11. Repeat steps 1 through 10 for all frequencies listed on the Test Record.

3-11 POWER LEVEL ACCURACY AND FLATNESS TESTS

The following tests can be used to verify that the 690XXA/691XXA meets its power level specifications. Power level verification testing is divided into two parts—power level accuracy tests and power level flatness tests.

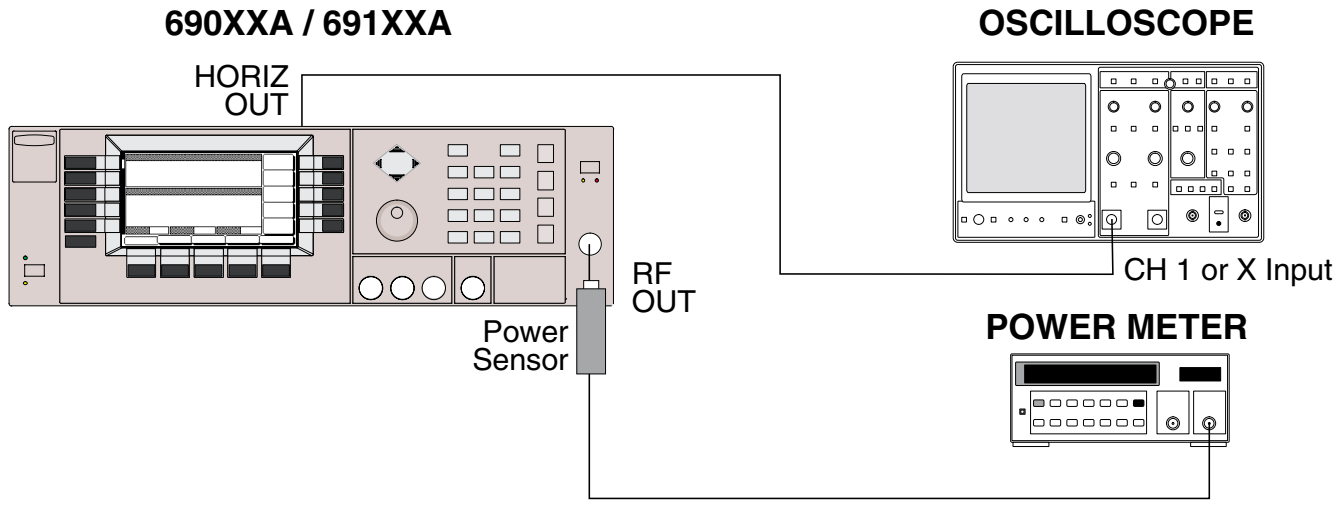

Figure 3-6. *Equipment Setup for Power Level Accuracy and Flatness Tests*

Test Setup

Connect the equipment, shown in Figure 3-6, as follows:

1. Calibrate the Power Meter with the Power Sensor.

2. Connect the Power Sensor to the RF OUTPUT of the 690XXA/691XXA.

NOTE

For ≤40 GHz models, use the K (male) to 2.4 mm (female) adapter to connect the Power Sensor to the RF OUTPUT connector.

3. Connect the 690XXA/691XXA rear panel HORIZ OUT to the Oscilloscope CH.1 input (X input).

NOTE

During this test it will be necessary to adjust the Power Meter's CAL FACTOR % setting as applicable for the frequency being tested.

Power Level Accuracy Test Procedure

Power level accuracy is tested by stepping the output power level down in 1 dB increments from its maximum rated power level and measuring the output power level at each step.

1. Set up the 690XXA/691XXA as follows:
   a. Reset the instrument by pressing **SYSTEM**, then Reset. Upon reset, the CW Menu is displayed.
   b. Press Edit F1 to open the current frequency parameter for editing.
   c. Set F1 to the CW frequency indicated on the Test Record.
   d. Press Edit L1 to open the current power level parameter for editing.
   e. Set L1 to the power level indicated on the Test Record.
2. Measure the output power level with the Power Meter and record the reading on the Test Record.
3. On the 690XXA/691XXA, use the cursor control key (diamond-shaped key) to decrement L1 to the next test power level on the Test Record. Measure and record the Power Meter reading on the Test Record.
4. Repeat step 3 for each of the test power levels listed on the Test Record for the current CW frequency.
5. Repeat steps 1 thru 4 for all CW frequencies listed on the Test Record.

Power Level Flatness Test Procedure

Power level flatness is tested by measuring the output power level variation during a full band sweep; first in the step sweep mode (690XXA/691XXA models), then in analog sweep mode (691XXA models only).

1. Set up the 690XXA/691XXA as follows for a step sweep power level flatness test:
   a. Reset the instrument by pressing **SYSTEM**, then Reset. The CW Menu is displayed.
   b. Press Step to place the instrument in the step sweep frequency mode and display the Step Sweep Menu.

c. With the Step Sweep Menu displayed, press the main menu key

FREQUENCY CONTROL

The Sweep Frequency Control Menu is then displayed.

d. Press Full to select a full range frequency sweep.

e. Press Edit L1 to open the current power level parameter for editing.

f. Set L1 to the power level indicated on the test record.

g. Now, return to the Step Sweep Menu by pressing the main menu key

CW/SWEEP SELECT

h. At the Step Sweep Menu, press Sweep Ramp to go to the Step Sweep Ramp Menu.

i. At this menu, press Dwell Time to open the dwell time-per-step parameter for editing.

j. Set the dwell time to 1 second.

NOTE
Monitor the 690XXA/691XXA's Horizontal Output on the Oscilloscope to determine sweep start and stop.

2. As the 690XXA/691XXA steps through the full frequency range, measure the maximum and minimum Power Meter readings and record the values on the Test Record. Verify that the variation (difference between the maximum and minimum readings) does not exceed the value noted on the Test Record.

NOTE
This concludes power level testing for series 690XXA CW generators. For series 691XXA sweep generators, continue on to step 3 to test power level flatness in the analog sweep mode.

3. Set up the 691XXA as follows for an analog sweep power level flatness test:
   a. Reset the instrument by pressing **SYSTEM**, then Reset. The CW Menu is displayed.
   b. Press Analog to place the 691XXA in the analog sweep frequency mode and display the Analog Sweep Menu.
   c. With the Analog Sweep Menu displayed, press the main menu key

      FREQUENCY CONTROL

      The Sweep Frequency Control Menu is then displayed.
   d. Press Full to select a full range frequency sweep.
   e. Press Edit L1 to open the current power level parameter for editing.
   f. Set L1 to the power level noted on the test record.
   g. Now, return to the Analog Sweep Menu by pressing the main menu key

      CW/SWEEP SELECT
   h. At the Analog Sweep Menu, press the menu soft-key Sweep Ramp to go to the Analog Sweep Ramp Menu.
   i. At this menu, press Sweep Time to open the sweep time parameter for editing.
   j. Set the sweep time to 99 seconds.

      NOTE
      Monitor the 691XXA's Horizontal Output on the Oscilloscope to determine sweep start and stop.

4. During the analog sweep, measure the maximum and minimum Power Meter readings and record the values on the Test Record. Verify that the variation (difference between the maximum and minimum readings) does not exceed the value noted on the Test Record.

Chapter 4
Calibration

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Chapter 4
Calibration

4-1 INTRODUCTION

This chapter contains procedures for calibrating the Series 690XXA/691XXA Synthesized CW/Sweep Generators. These procedures are typically performed because out-of-tolerance conditions have been noted during performance verification testing (see Chapter 3) or as a result of replacement of subassemblies or RF components.

NOTE

The calibration procedures herein support operating firmware versions as follows: series 690XXA models–Version 1.00 and above; series 691XXA models–Version 1.00 and above. It is recommended that you upgrade your instrument's operating firmware to the latest ava bilable version prior to calibration.

4-2 RECOMMENDED TEST EQUIPMENT

Table 4-1 (page 4-4) provides a list of the recommended test equipment for these calibration procedures.

The procedures refer to specific test equipment front panel control settings when the test setup is critical to making accurate measurements. In some cases, the user may substitute test equipment having the same critical specifications as those on the recommended test equipment list.

Contact your local ANRITSU service center (Refer to Table 1-5 on page 1-18) if you need clarification of any equipment or procedural reference.

4-3 TEST RECORDS

A blank copy of a sample calibration test record for each 690XXA/691XXA model is provided in Appendix A. Each test record contains model-specific variables called for by the calibration procedures. It also provides a means for maintaining an accurate and complete record of instrument calibration. We recommend that you copy these pages and use them to record the results from (1) your initial calibration of out-of-tolerance 690XXA/691XXA circuits, or (2) your initial calibration of the 690XXA/691XXA following replacement of subassemblies or RF components. These initial readings can be used later as benchmark values for future tests of the same serial-numbered instruments.

4-4 CALIBRATION FOLLOWING SUBASSEMBLY REPLACEMENT

Table 4-2 (page 4-6) lists the calibration that should be performed following the replacement of 690XXA/691XXA subassemblies or RF components.

4-5 CONNECTOR AND KEY LABEL NOTATION

The calibration procedures include many references to equipment interconnections and control settings. For all 690XXA/691XXA references, specific labels are used to denote the appropriate menu key, data entry key, data entry control, or connector (such as CW/SWEEP SELECT or RF OUTPUT). Most references to supporting test equipment use general labels for commonly used controls and connections (such as Span or RF Input). In some cases, a specific label is used that is a particular feature of the test equipment listed in Table 4-1.

Table 4-1. *Recommended Test Equipment for Calibration Procedures (1 of 2)*

INSTRUMENT	CRITICAL SPECIFICATION	RECOMMENDED MANUFACTURER/MODEL	PROCEDURE NUMBER
Frequency Counter	*Frequency Range:* 1 to 20 GHz *Input Impedance:* 50Ω *Resolution:* 1 Hz	EIP Microwave, Inc. Model 578B	4-7
Spectrum Analyzer	*Frequency Range:* 1 to 5 GHz *Resolution Bandwidth:* 10 Hz	Tektronix, Model 2794	4-13
Power Meter with Power Sensor	*Power Range:* –30 to +20 dBm (1μW to 100 mW)	Hewlett-Packard Model 437B, with Power Sensor: HP 8487A (0.01 to 50 GHz)	4-12
Power Meter with Power Sensor	*Power Range:* –30 to +20 dBm (1μW to 100mW)	ANRITSU ML4803A, with Power Sensor: MP716A4 (50 to 75 GHz)	4-12
Frequency Standard	*Frequency:* 10 MHz *Accuracy:* 1×10^{-10} parts/day	Spectracom Corp., Model 8161	4-7
Function Generator	*Output Voltage:* 2 volts peak-to-peak *Functions:* 0.4 Hz to 100 kHz sine and square waveforms	Hewlett-Packard, Model 8116A	4-12, 4-13
Function Generator	*Output Voltage:* 2 volts peak-to-peak *Functions:* 0.4 Hz to 100 kHz sine and square waveforms	Hewlett-Packard, Model 33120A	4-12. 4-13
Digital Multimeter	*Resolution:* 4-1/2 digits (to 20V) *DC Accuracy:* 0.002% +2 counts *DC Input Impedance:* 10 MΩ *AC Accuracy:* 0.07% +100 counts (to 20 kHz) *AC Input Impedance:* 1 MΩ	John Fluke, INC., Model 8840A, with Option 8840A-09K (True RMS AC)	4-12, 4-13

Table 4-1. *Recommended Test Equipment for Calibration Procedures (2 of 2)*

INSTRUMENT	CRITICAL SPECIFICATION	RECOMMENDED MANUFACTURER/MODEL	PROCEDURE NUMBER
Scalar Network Analyzer, with RF Detector	*Frequency Range:* 0.01 to 60 GHz	ANRITSU Model 562, with RF Detector: 560-7K50 (0.01 to 40 GHz) 560-7VA50 (0.01 to 50 GHz) SC5198 (40 to 60 GHz)	4-8, 4-10
Adapter	K (male) to 2.4 mm (female) Adapts the Power Sensor, HP 8487A, to the 690XXA/691XXA RF OUTPUT connector (≤40 GHz models)	Hewlett-Packard Part Number: HP 11904D	4-12
Adapter	Adapts the MP716A4 Power Sensor to the ML4803A Power Meter	ANRITSU MA4002B	4-12
Adapter	WR15 to V (male) Adapts the MP716A4 Power Sensor to the 690XXA/691XXA RF OUTPUT connector (>40 GHz models)	ANRITSU, Model 35WR15V	4-12
Attenuator	*Frequency Range:* DC to 40 GHz *Max Input Power:* >+17 dBm *Attenuation:* 10 dB	ANRITSU, Model 41KC-10	4-8, 4-10
Attenuator	*Frequency Range:* DC to 60 GHz *Max Input Power:* >+17 dBm *Attenuation:* 10 dB	ANRITSU, Model 41V--10	4-8, 4-10
Personal Computer	*PC Configuration:* IBM AT or compatible *Operating System:* Windows 3.1 *Accessories:* Mouse	Any common source	All procedures
Serial Interface Assy	Provides serial interface between the PC and the 690XXA/691XXA.	ANRITSU P/N: T1678	All procedures
Tee	*Connectors:* 50Ω BNC	Any common source	4-12, 4-13
Cables	*Connectors:* 50Ω BNC	Any common source	All procedures

Table 4-2. *Calibration Following Subassembly/RF Component Replacement*

Subassembly/RF Component Replaced	Perform the Following Calibration(s) in Paragraph(s):
A1, A2 Front Panel Assy	None
A3 Reference Loop PCB	4-7
A4 Coarse Loop PCB	4-7
A5 Fine Loop PCB	4-7
A6 Square Wave Generator PCB	None
A7 YIG Loop PCB	None
A9 PIN Control PCB	4-8, 4-9, 4-10, 4-11
A10 ALC PCB	4-8, 4-9, 4-10, 4-11, 4-12
A11 FM PCB	4-13
A12 Analog Instruction PCB	4-7
A13 YIG Driver PCB	4-7
A14 SDM, SQM Driver PCB	4-9, 4-10, 4-11
A15 Regulator PCB	None
A16 CPU Interface PCB	None
A17 CPU PCB	4-8 thru 4-13. None, if calibration EEPROM reused.
A18 Power Supply PCB	None
A19 AC Line Conditioner PCB	None
A21 Line Filter/Rectifier PCB	None
A21-1 or A21-2 BNC/Aux I/O Connector PCB	None
YIG-tuned Oscillator	4-7
0.01 to 2 GHz Down Converter Assy	4-8, 4-9, 4-10, 4-11
0.5 to 2.2 GHz Digital Down Converter Assy	4-8, 4-9, 4-10, 4-11
Switched Filter Assy	4-8, 4-9, 4-10, 4-11
Switched Doubler Module (SDM)	4-8, 4-9, 4-10, 4-11
Source Quadrupler Module (SQM)	4-8, 4-9, 4-10, 4-11
Forward Coupler	4-8, 4-9, 4-10, 4-11
Directional Coupler	4-8, 4-9, 4-10, 4-11
Step Attenuator	4-8, 4-9, 4-10

4-6 INITIAL SETUP

The 690XXA/691XXA is calibrated using an IBM compatible PC and external test equipment. The PC must have the Windows 3.1 or Windows 95 operating system installed and be equipped with a mouse. Initial setup consists of interfacing the PC to the 690XXA/691XXA.

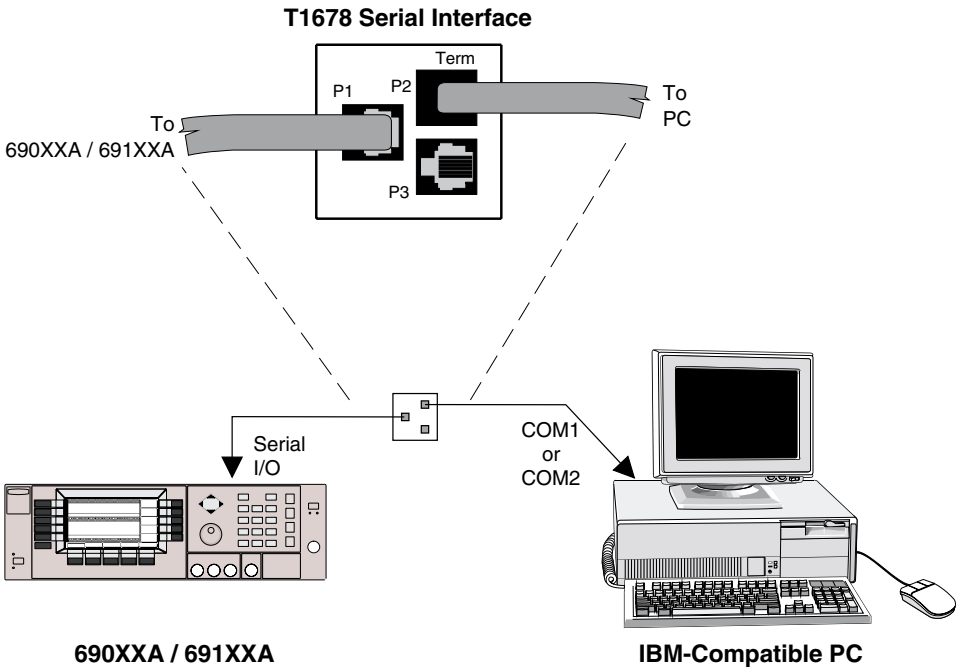


Figure 4-1. *PC to 690XXA/691XXA Interconnection for Calibration*

Interconnection

Using the ANRITSU P/N T1678 serial interface assembly, connect the PC to the 690XXA/691XXA as follows:

1. Connect the wide flat cable between the 690XXA/691XXA rear panel SERIAL I/O connector and the P1 connector on the T1678 serial interface PCB.

2. Connect the narrow flat cable between the P2 (TERM) connector on the T1678 serial interface PCB and the COM1 or COM2 connector on the PC. Use the RJ11-to-DB-9 or RJ11-to-DB-25 adapter, provided with the T1678 serial interface assembly, to make the connection at the PC.

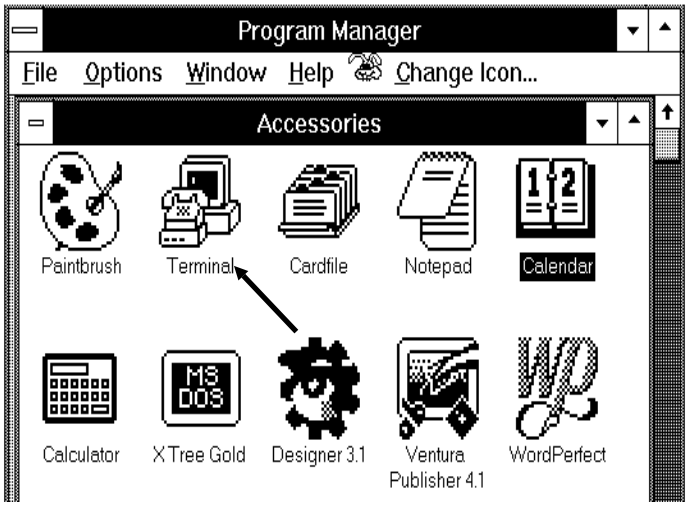
PC Setup — Windows 3.1

Configure the PC with Windows 3.1 operating system to interface with the 690XXA/691XXA as follows:

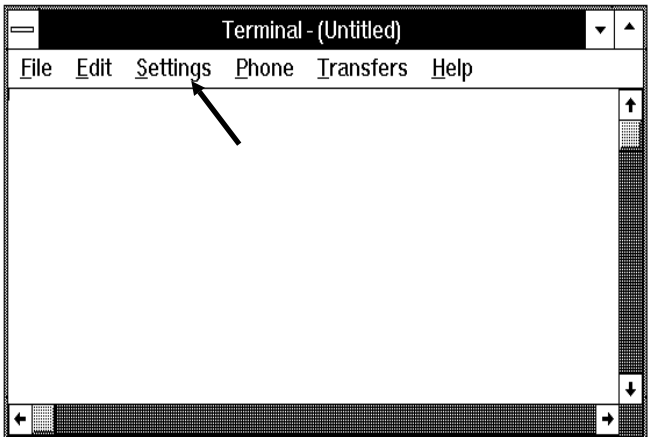
1. Power up the 690XXA/691XXA.

2. Power up the PC and place in Windows.

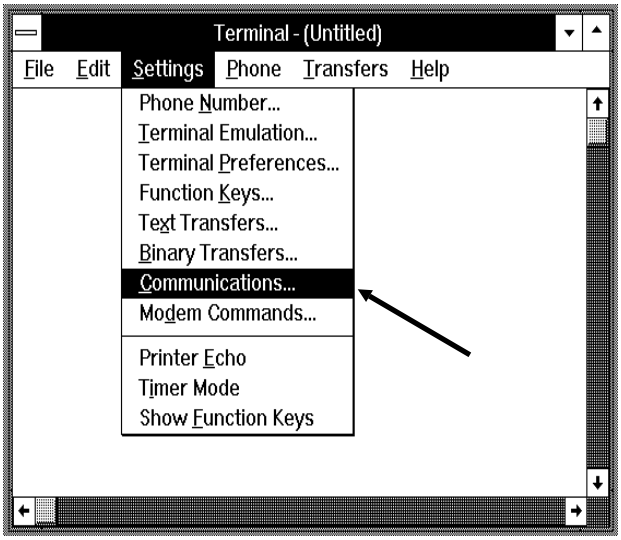
3. Double click on the Terminal Icon to bring up the Terminal (Untitled) window. The initial installation of Windows places the Terminal Icon in the Accessories window.



4. At the Terminal window, click on Settings to display the Settings menu.

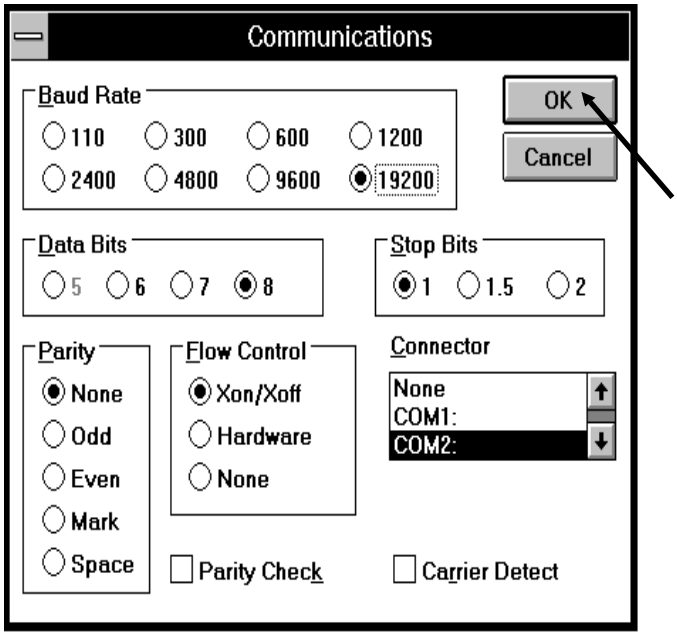


5. Click on Communications.



6. At the Communications Dialog box, select the following options:

Baud Rate	19200
Data Bits	8
Stop Bits	1
Parity	None
Flow Control	Xon/Xoff
Connector	Select connection made during interconnection



7. After making the selections, click on the OK button.

8. Press <ENTER> on the keyboard.

9. Verify that a **$** prompt appears on the PC display.

10. This completes the initial setup for calibration.

PC Setup — Windows 95

Configure the PC with Windows 95 operating system to interface with the 690XXA/691XXA as follows:

1. Power up the 690XXA/691XXA.

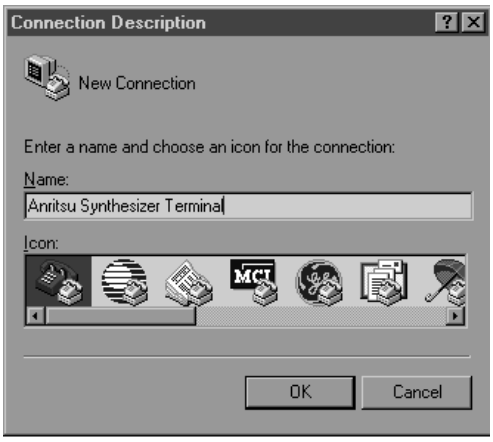
2. Power up the PC and place it in Windows.

3. Click the Start button to activate the first menu.

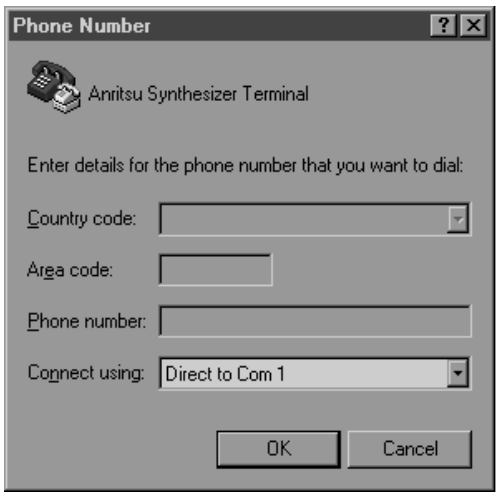
4. Go to Programs and place the mouse pointer on Accessories to highlight the third menu.

5. Select Hyper Terminal to bring up the selection window (below).

6. Click on Hypertrm (Hypertrm.exe) to bring up the New Connection window (next page).

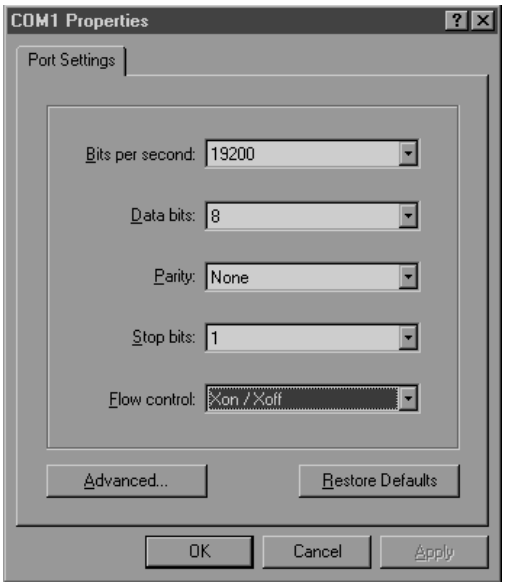


7. In the New Connection Name box, type a name for the connection, then click on the OK button. The window below is now displayed.



8. In the Connect using box, type: **`Direct to Com"_"`**. Enter the number of the communications port being used, for example: Com 1.

9. Click on OK. The Communications Port Properties window is displayed (next page).



10. In the Properties window, make the following selections:

Bits per second	19200
Data bits	8
Parity	None
Stop bits	1
Flow control	Xon / Xoff

11. After making the selections, click on the OK button.

12. Press <ENTER> on the keyboard.

13. Verify that the **$** prompt appears on the PC display.

14. This completes the initial setup for calibration.

4-7 PRELIMINARY CALIBRATION

This procedure provides the steps necessary to initially calibrate the coarse loop, fine loop, frequency instruction, and internal DVM circuitry and the 100 MHz reference oscillator of the 690XXA/691XXA.

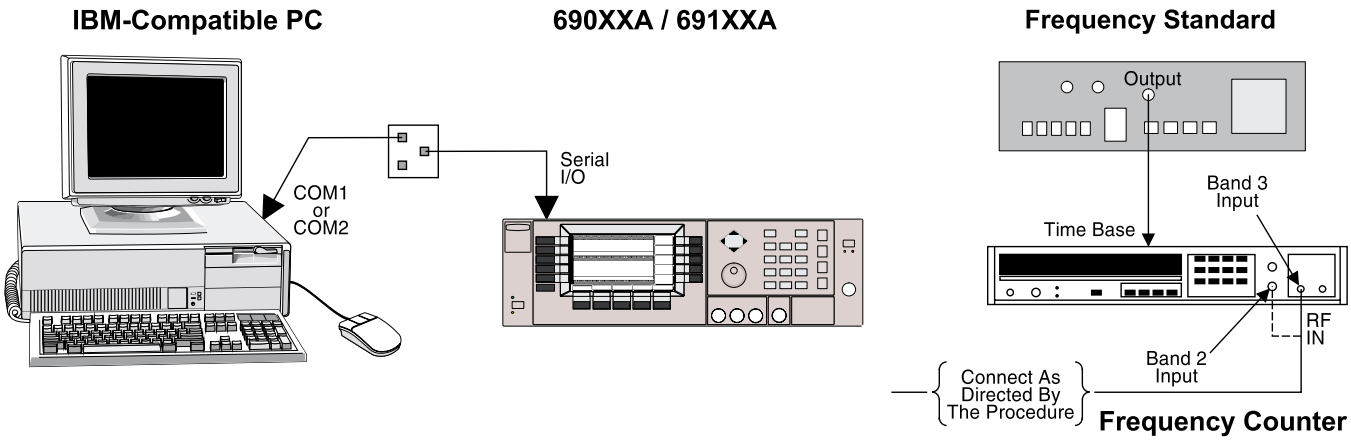


Figure 4-2. *Equipment Setup for Preliminary Calibration*

Equipment Setup

Connect the equipment, shown in Figure 4-2, as follows:

1. Interface the PC to the 690XXA/691XXA by performing the initial setup procedure, pages 4-7 to 4-12.

2. Connect the Frequency Counter to the 690XXA/691XXA when directed to do so during the calibration procedure.

NOTE

If the 690XXA/691XXA has option 19 installed, verify that the GPIB is configured for the Native external interface language before beginning instrument calibration.

Before beginning this calibration procedure, *always* let the 690XXA/691XXA warm up for a minimum of one hour.

Calibration Steps

Each of the steps in this procedure provides initial calibration of a specific 690XXA/691XXA circuit or component. To ensure accurate instrument calibration, each step of this procedure must be performed in sequence.

1. Calibrate the internal DVM circuitry as follows:
   a. At the **$** prompt, type: **calterm 119** and press <ENTER>. (The **$** prompt will appear on the screen when the calibration is complete.)
   b. Record step completion on the Test Record.

2. Calibrate the Fine Loop Pretune DAC as follows:
   a. At the **$** prompt, type: **calterm 136** and press <ENTER>. (The **$** prompt will appear on the screen when the calibration is complete.)
   b. Record step completion on the Test Record.

3. Calibrate the Sweep Time DAC as follows:
   a. At the **$** prompt, type: **calterm 132** and press <ENTER>. (The **$** prompt will appear on the screen when the calibration is complete.)
   b. Record step completion on the Test Record.

4. Calibrate the YIG Frequency Offset DAC as follows:
   a. At the **$** prompt, type: **calterm 134** and press <ENTER>.
   b. Follow the instructions on the screen.

   NOTE
   Adjust the DAC to the number that will get the closest to the frequencies of 1.9 GHz and 8.3 GHz called for by the procedure.

   c. Record step completion on the Test Record.

5. Calibrate the YIG Frequency Linearizer DACs as follows:
   a. At the **$** prompt, type: **calterm 127** and press <ENTER>.
   b. Follow the instructions on the screen. Enter the value of the frequency counter reading as XXXX MHz.
   c Record step completion on the Test Record.

NOTE
To save the calibration data after completing any calibration step, type: **calterm 787** and press <ENTER>.

NOTE

Because the 100 MHz Calibration DAC is an 8-bit DAC, adjustment resolution is typically 400 Hz/step.

6. Calibrate the 100 MHz Reference Oscillator as follows:
   a. If Option 16 (High Stability Time Base) is installed, disconnect the cable at A3J6.
   b. Connect the frequency counter to the 690XXA/691XXA RF output connector .
   c. At the **$** prompt, type: **calterm 130** and press <ENTER>.
   d. Follow the instructions on the screen.
   e. Reconnect the cable to A3J6, if removed.
   f. If Option 16 is installed, use a Phillips screwdriver and remove the screw on top of the 10 MHz High Stability Crystal Oscillator assembly to gain access the timebase adjustment screw.
   g. Using a Phillips screwdriver, adjust the timebase to obtain a frequency counter reading of exactly 10 GHz.
   h. Record step completion on the Test Record.
7. Calibrate the Ramp Center DAC as follows:
   a. At the **$** prompt, type: **calterm 129** and press <ENTER>. (The **$** prompt will appear on the screen when the calibraton is complete.)
   b. Record step completion on the Test Record.
8. Calibrate the Sweep Width DAC as follows:
   a. At the **$** prompt, type: **calterm 133** and press <ENTER>. (This calibration can take approximately 2 minutes to complete.)

      The **$** prompt will appear on the screen when the calibration is complete.
   b. Record step completion on the Test Record.
9. Calibrate the Center Frequency DAC as follows:
   a. At the **$** prompt, type: **calterm 114** and press <ENTER>. (The **$** prompt will appear on the screen when the calibration is complete.)
   b. Record step completion on the Test Record.

CAUTION

When saving calibration data, turning off the instrument before the **$** prompt returns to the screen can cause all stored data to be lost.

10. Store the calibration data as follows:
    a. At the **$** prompt, type: **`calterm 787`** and press <ENTER>. (The **$** prompt will appear on the screen when the calibration data has been stored.)
    b. Record step completion on the Test Record.

4-8 SWITCHED FILTER SHAPER CALIBRATION

This procedure provides the steps necessary to adjust the Switched Filter Shaper Amplifier gain to produce a more constant level amplifier gain with power level changes.

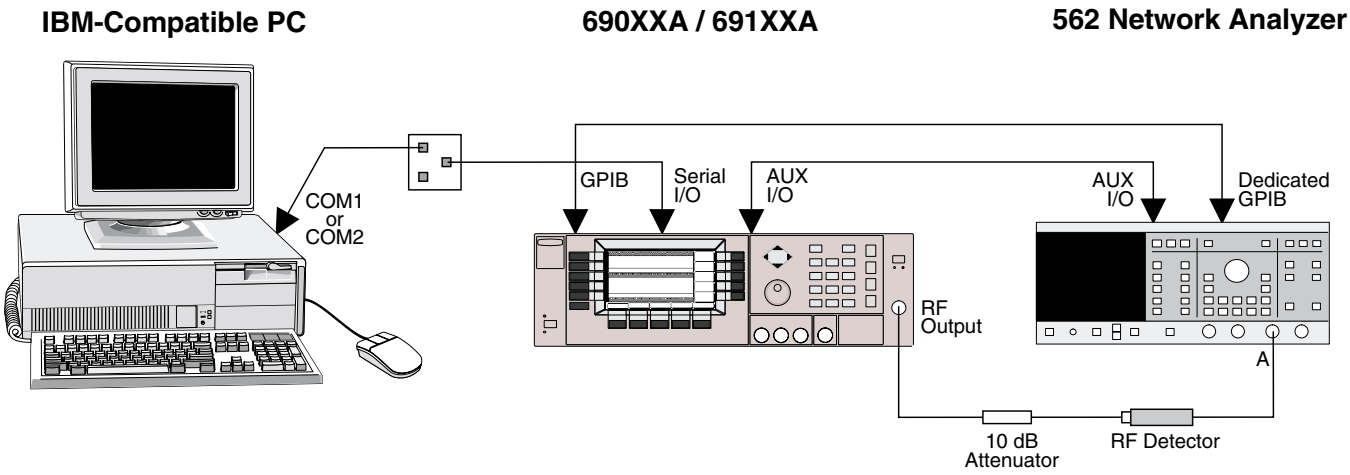


Figure 4-3. *Equipment Setup for Switched Filter Shaper Calibration*

Equipment Setup

Connect the equipment, shown in Figure 4-3, as follows:

1. Interface the PC to the 690XXA/691XXA by performing the initial setup procedure, pages 4-7 to 4-12.

2. Using the Auxiliary I/O cable, connect the 690XXA/691XXA rear panel AUX I/O connector to the 562 Network Analyzer AUX I/O connector.

3. Using the GPIB cable, connect the 562 Network Analyzer DEDICATED GPIB connector to the 690XXA/691XXA IEEE-488 GPIB connector.

4. Connect the RF Detector to the 562 Network Analyzer Channel A Input connector.

5. Connect the 690XXA/691XXA RF OUTPUT connector to the RF Detector via a 10 dB Attenuator.

NOTE

Before beginning this calibration procedure, *always* let the 690XXA/691XXA warm up for a minimum of one hour.

Log Amplifier Zero Calibration

Before the Switched Filter Shaper Amplifier can be adjusted, zero calibration of the ALC Log amplifier must performed to eliminate any DC offsets.

1. Perform ALC Log amplifier zero calibration as follows:
   a. At the **$** prompt on the PC display, type: **calterm 115** and press <ENTER>

      The **$** prompt will appear on the screen when ALC Log amplifier zero calibration is complete. (This can take up to 3 minutes for a 40 GHz unit.)

   b. Record step completion on the Test Record.

NOTE

The following Limiter DAC adjustment procedure applies only to 690XXA/ 691XXAs with Option 15A (High Power Output). If your instrument does not have this option, go directly to the Shaper DAC adjustment procedure.

Limiter DAC Adjustment

The following steps in the procedure let you adjust the Switched Filter Limiter DAC which controls the maximum gain of the Switched Filter Shaper Amplifier. Each frequency band will be scanned for the maximum unleveled power point before adjustment of the Limiter DAC to ensure that the Shaper Amplifier is not driven to saturation.

1. Set up the 562 Network Analyzer as follows:
   a. Press the System Menu key.
   b. From the System Menu display, select RESET.
   c. Press CHANNEL 2 DISPLAY: OFF.
   d. Press CHANNEL 1 DISPLAY: ON.
   e. Press CHANNEL 1 MENU key.
   f. From the Channel 1 Menu display, select POWER.
   g. Press OFFSET/RESOLUTION.
   h. Set Resolution to 5 dB/Div.
   i. Adjust Offset to center the display.

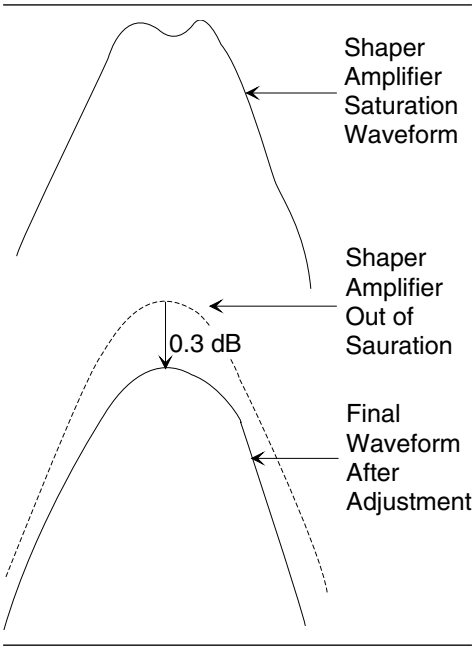


Figure 4-4. *Limiter DAC Adjustment Waveforms*

2. Adjust the Switched Filter Limiter DAC for each of the frequency bands as follows:
   a. At the **$** prompt on the PC display, type: **`calterm 145`** and press <ENTER>.
   b. On the 562 Network Analyzer, set the Resolution to 0.2 dB and adjust the offset to center the top of the triangle waveform on the display.
   c. Observe the displayed waveform to determine whether the Shaper Amplifier is being driven to saturation. This is indicated by a dip in the top of the triangle waveform (Figure 4-4).

      If the displayed waveform indicates there is not saturation, proceed to step e. If there is a dip in the waveform, go to step d.
   d. On the computer keyboard, use 8, 9, or 0 to decrement the value of the DAC's setting until the top of the triangle waveform starts to become rounded (Shaper Amplifier is no longer being driven to saturation). Continue decrementing until the top of the waveform is 0.3 dB below this point.
   e. Press **Q** on the keyboard to go to the next frequency band.
   f. Repeat steps b thru e until the DAC has been checked and adjusted for all frequency bands.
   g. Press **Q** on the keyboard to exit the program. (The **$** prompt will appear on the screen.)
   h. Record step completion on the Test Record.

Shaper DAC Adjustment

For Models 690XXA with Firmware Versions 1.00 to 1.17; Models 691XXA with Firmware Versions 1.00 to 1.22; Models 690X5A with Firmware Versions 1.00 to 1.17; and Models 691X5A with Firmware Versions 1.00 to 1.20.

NOTE

The 10 dB attenuator between the 690XXA/691XXA RF OUTPUT connector and the RF Detector may not be required for frequencies >20 GHz.

The following steps in the procedure lets you adjust the Switched Filter Shaper DAC which controls the gain of the Switched Filter Shaper Amplifier. Each frequency band will be scanned for the minimum unleveled power point before adjustment of the shaper DAC.

1. Set up the 562 Network Analyzer as follows:
   a. Press the System Menu key.
   b. From the System Menu display, select RESET.

c. Press CHANNEL 2 DISPLAY: OFF.

d. Press CHANNEL 1 DISPLAY: ON.

e. Press CHANNEL 1 MENU key.

f. From the Channel 1 Menu display, select POWER.

g. Press OFFSET/RESOLUTION.

b. Set Resolution to 5 dB/Div.

c. Adjust Offset to center the display.

2. Adjust the Switched Filter Shaper DAC for each of the frequency bands as follows:

   a. At the **$** prompt on the PC display, type: **`calterm 138`** and press <ENTER>.

   NOTE
   At the start of each frequency band, there will be a delay while the minimum unleveled power point is determined.

   b. On the computer keyboard, use 1, 2, or 3 to increment and 8, 9, or 0 to decrement the value of the DAC's setting to adjust the triangle waveform being displayed on the 562 Network Analyzer (Figure 4-5) for the most linear response.

   There will be a delay while the amplifier compression point is determined and after each key stroke as the DAC is adjusted.

   c. When the DAC has been adjusted for the current frequency band, press **Q** on the keyboard to go to the next frequency band.

   d. Repeat steps b. and c. until the DAC has been adjusted for all frequency bands.

   e. Press **Q** on the keyboard to exit the program. (The **$** prompt will appear on the screen.)

   f. Record step completion on the Test Record.

3. Store the calibration data in non-volatile memory (EEPROMs) on the A17 CPU PCB as follows:

   a. Type: **`calterm 787`** and press <ENTER>. (The **$** prompt will appear on the screen when the data has been stored.)

   b. Record step completion on the Test Record.

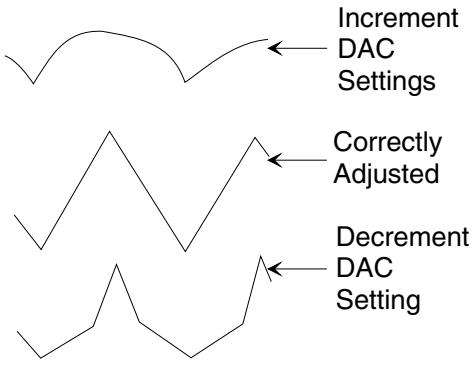


Figure 4-5. *Shaper DAC Adjustment Waveform Examples*

CAUTION

When saving calibration data, turning off the instrument before the **$** prompt returns to the screen can cause all stored data to be lost.

Shaper DAC Adjustment

For Models 690XXA with Firmware Version 1.19 and above; Models 691XXA with Firmware Version 1.24 and above, Models 690X5A with Firmware Version 1.19 and above; and Models 691X5A with Firmware Version 1.22 and above.

The following step in the procedure adjusts the Switch Filter Shaper DAC which controls the gain of the Switched Filter Shaper Amplifier. Each frequency band will be scanned for the minimum unleveled power point before automatic adjustment of the shaper DAC.

1. At the **$** prompt on the PC display, type: **`calterm 138`** and press <ENTER>. (The **$** prompt will appear on the screen when the calibration is complete.)

NOTE

The calibration routine may take up to 20 minutes depending on the frequency range of the 690XXA/691XXA being calibrated.

CAUTION

When saving calibration data, turning off the instrument before the **$** prompt returns to the screen can cause all stored data to be lost.

2. Store the calibration data in non-volatile memory (EEPROMs) on the A17 CPU PCB as follows:
   a. Type: **`calterm 787`** and press <ENTER>. (The **$** prompt will appear on the screen when the data has been stored.)
   b. Record step completion on the Test Record.

4-9 RF LEVEL CALIBRATION

RF level calibration requires the use of an automated test system. A computer-controlled power meter measures the 690XXA/691XXA power output at many frequencies throughout the frequency range of the instrument. Correction factors are then calculated and stored in non-volatile memory (EEPROM) located on the A17 CPU PCB.

This calibration is required following replacement of either the A9 PIN Control PCB, the A10 ALC PCB, the A14 SDM, SQM Driver PCB, the Switched Filter Assembly, the 0.01 to 2 GHz Down Converter Assembly, the 0.5 to 2.2 GHz Digital Down Converter Assembly, the Switched Doubler Module (SDM), the Source Quadrupler Module (SQM), the Forward Coupler, the Directional Coupler, or the Step Attenuator.

The RF level calibration software is available from ANRITSU by ordering:

- Part number 2300-104, Version 2.0 and above, for all ≤50 GHz 690XXA/691XXA models.
- Part number 2300-209, Version 1.0 and above, for 60 GHz and 65 GHz 690XXA/691XXA models.

This calibration program warrants level accuracy specifications from maximum power to –70 dBm. For calibration below –70 dBm, the 690XXA/691XXA must be returned to your ANRITSU service center for calibration. The RF level calibration software comes on a 3.5-inch/ 1.44 Mbyte, MS-DOS formatted floppy disk.

For information concerning test equipment requirements and ordering the automated program, contact your ANRITSU service center (refer to Table 1-5 on page 1-18).

4-10 ALC SLOPE CALIBRATION (691XXA ONLY)

This procedure provides the steps necessary to perform ALC Slope calibration. The ALC Slope is calibrated to adjust for decreasing output power-vs-output frequency in full band analog sweep.

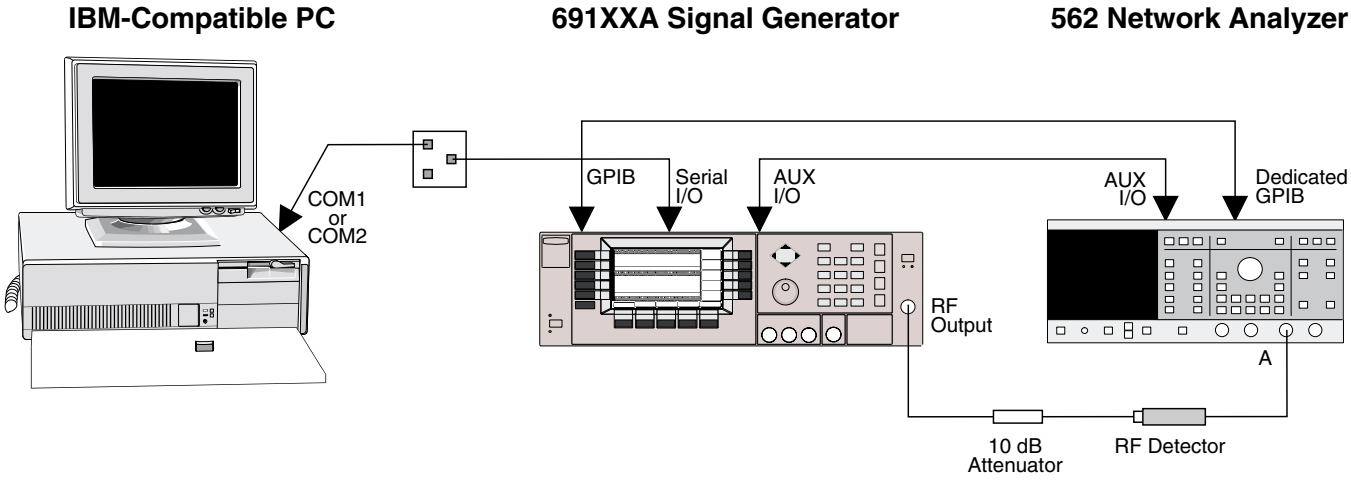


Figure 4-6. *Equipment Setup for ALC Slope Calibration*

Equipment Setup

Connect the equipment, shown in Figure 4-6, as follows:

1. Interface the PC to the 691XXA by performing the initial setup procedure, pages 4-7 to 4-12.
2. Using the Auxiliary I/O cable, connect the 691XXA rear panel AUX I/O connector to the 562 Network Analyzer AUX I/O connector.
3. Using the GPIB cable, connect the 562 Network Analyzer DEDICATED GPIB connector to the 691XXA IEEE-488 GPIB connector.
4. Connect the RF Detector to the 562 Network Analyzer Channel A Input connector.
5. Connect the 691XXA RF OUTPUT connector to the RF Detector via a 10 dB Attenuator.

NOTE

Before beginning this calibration procedure, always let the 691XXA warm up for a minimum of one hour.

ALC Slope DAC Adjustment

The following procedure lets you adjust the ALC Slope over individual frequency ranges to compensate for decreasing output power-vs-frequency in analog sweep.

NOTE

For 691X5A models, the frequency ranges for Band 0 and Band 1 are 0.5 to 2.2 GHz and 2.2 to 8.4 GHz respectively.

The procedure begins by letting you adjust the ALC Slope for band 0 (0.01 to 2.0 GHz), if installed. It then continues letting you adjust the ALC Slope from 2 GHz to the top frequency of the instrument in up to four bands. The band frequency ranges are:

Band 1	2.0 to 8.4 GHz
Band 2	8.4 to 20 GHz
Band 3	20.0 to 40.0 GHz (or 26.5 GHz)
Band 4	40.0 to 65.0 GHz

During band 1 thru 3/4 ALC Slope adjustment, the 562 Network Analyzer display (Figure 4-7) shows the response from 2 GHz to the top frequency of the model, as adjustment is done band by band.

1. Set up the 562 Network Analyzer as follows:
   a. Press the System Menu key.
   b. From the System Menu display, select RESET.
   c. Press CHANNEL 2 DISPLAY: OFF.
   d. Press CHANNEL 1 DISPLAY: ON.
   e. Press CHANNEL 1 MENU key.
   f. From the Chanel 1 Menu Display, select TRANSMISSION and SELECT INPUT (NON-RATIO A).

2. Set up the 691XXA as follows:
   a. Reset the instrument by pressing **SYSTEM** then Reset. Upon reset the CW Menu is displayed.
   b. Press Step. The Step Sweep Menu is displayed.
   c. Press **FREQUENCY CONTROL**, then Full to select the full frequency range of the unit being calibrated.

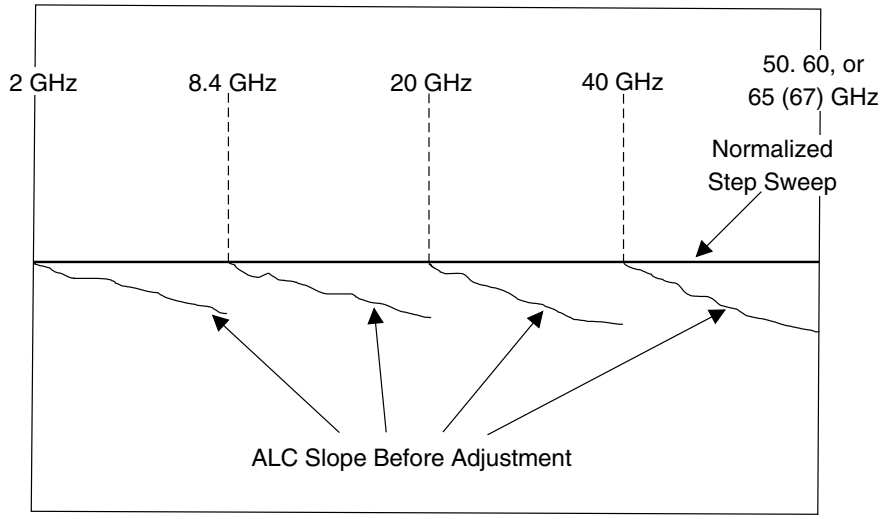


Figure 4-7. *ALC Slope Adjustment Waveform Display*

d. Press **CW/SWEEP SELECT** to return to the Step Sweep Menu display.

e. Press Sweep Ramp. At the resulting Step Sweep Ramp Menu, press Num of Steps and set the number of steps to 400.

3. Make the following selections on the 562 Network Analyzer to normalize the step sweep.

   a. Press CALIBRATION and follow the menu on the display.

   b. Press AUTOSCALE.

   c. Press OFFSET/RESOLUTION and set the Resolution to 0.5 dB.

4. On the 691XXA, press Analog to select the analog sweep mode.

5. Adjust the ALC Slope as follows:

   a. At the **$** prompt on the PC display, type: **slpcal** and press <ENTER>.

   On the computer keyboard, the adjustment keys are:

Slope (all bands)	**E** (Up)	**D** (Down)
Offset (band 1-4 only)	**Q** (Up)	**A** (Down)

b. Adjust the ALC Slope so that the power at the start and stop frequencies (of the analog sweep for band 0) match as closely as possible the normalized straight line in step sweep mode. When completed, press **n** for the next band.

c. Using the Slope and Offset adjustment keys, continue until the ALC Slope for all bands has been adjusted.

d. Type: **x** and press <ENTER> to exit the calibration routine. (The **$** prompt will appear on the screen.)

e. Record step completion on the Test Record.

6. Store the new DACs setting values in non-volatile memory (EEPROMs) on the A17 CPU PCB as follows:

a. Type: **calterm 787** and press <ENTER>. (The **$** prompt will appear on the screen when the data has been stored.)

b. Record step completion on the Test Record.

CAUTION

When saving calibration data, turning off the instrument before the **$** prompt returns to the screen can cause all stored data to be lost.

4-11 ALC BANDWIDTH CALIBRATION

This procedure provides the steps necessary to perform ALC Bandwidth calibration. The ALC Bandwidth is adjusted to compensate for gain variations of the modulator. The adjustment is performed for each frequency band. This provides a more consistent bandwith throughout the frequency range of the instrument.

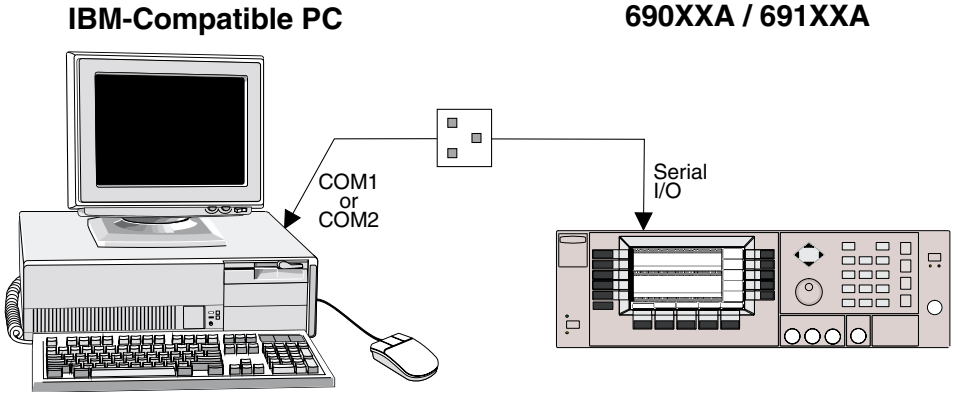


Figure 4-8. *Equipment Setup for ALC Bandwidth Calibration*

Equipment Setup

Connect the equipment, shown in Figure 4-8, as follows:

1. Interface the PC to the 690XXA/691XXA by performing the initial setup procedure, pages 4-7 to 4-12.

NOTE

Before beginning this calibration procedure, *always* let the 690XXA/691XXA warm up for a minimum of one hour.

Bandwidth Calibration

The following procedure lets you (1) calibrate the ALC bandwith and (2) store the calibration data in non-volatile memory (EEPROMs) on the A17 CPU PCB.

1. Enter the ALC Bandwidth calibration routine as follows:
   a. At the **$** prompt on the PC display, type: **`calterm 110`** and press <ENTER>.

   The $ prompt will appear on the screen when the ALC Bandwidth calibration is complete. (This can take up to 15 minutes depending on the frequency range of the 690XXA/691XXA.)

b. Record step completion on the Test Record.

2. Store the calibration data as follows:

   a. At the **$** prompt, type: **calterm 787** and press <ENTER>. (The **$** prompt will appear on the screen when the calibration data has been stored.)

   b. Record step completion on the Test Record.

CAUTION

When saving calibration data, turning off the instrument before the **$** prompt returns to the screen can cause all stored data to be lost.

4-12 AM CALIBRATION (691XXA ONLY)

This procedure provides the steps necessary to perform AM calibration. This consists of calibrating the AM Calibration DAC and the AM Meter circuit. The AM Calibration DAC is calibrated for input sensitivities of 100%/V (linear mode) and 25 dB/V (logarithmic mode) for frequencies ≤2 GHz and >2 GHz (≤2.2 GHz and >2.2 GHz for 691X5A models).

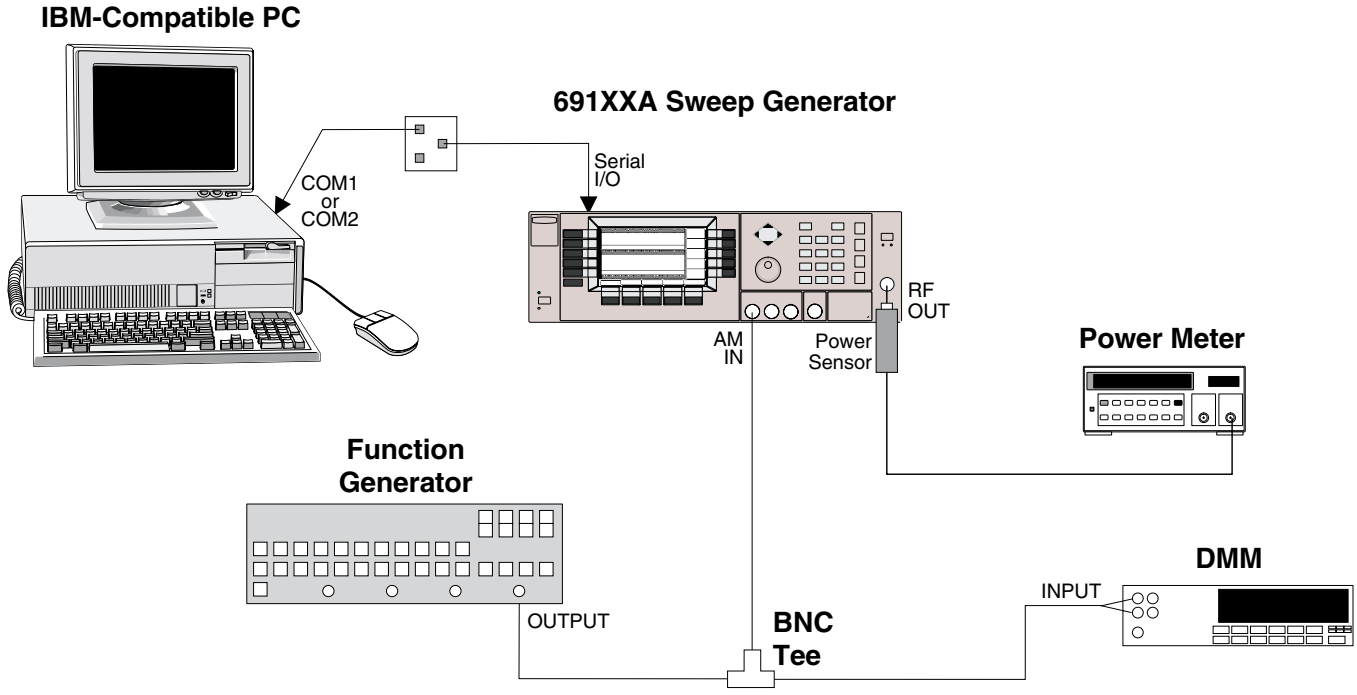


Figure 4-9. *Equipment Setup for AM Calibration*

Equipment Setup

Connect the equipment, shown in Figure 4-9, as follows:

1. Interface the PC to the 691XXA by performing the initial setup procedure, pages 4-7 to 4-12.
2. Connect the Function Generator Output to the BNC tee. Connect one leg of the tee to the 691XXA front panel AM IN. Connect the other leg of the tee to the DMM input.
3. Calibrate the Power Meter with the Power Sensor.

4. Connect the Power Sensor to the RF OUTPUT of the 691XXA. (For ≤40 GHz models, use the K (male) to 2.4 mm (female) adapter.)

NOTE
Before beginning this calibration procedure, always let the 691XXA warm up for a minimum of one hour.

AM Calibration Procedure

The following procedure let you (1) adjust the AM Calibration DAC to provide the correct amount of AM in both linear (100%/V sensitivity) and log (25 dB/V sensitivity) modes of operation for frequencies of ≤2 GHz and >2 GHz, (2) calibrate the AM Meter circuit, and (3) store the results in non-volatile memory (EEPROM) on the A17 CPU PCB.

NOTE
For 691X5A models, the procedure for Linear AM and Log AM calibration must also be performed twice—once for frequencies of 2.2 GHz and once for frequencies of

NOTE
For those instruments that contain a Down Converter, the procedure for Linear AM and Log AM calibration must be performed twice—once for frequencies ≤2 GHz and once for frequencies >2 GHz. Upon initial completion of each procedure, the program will automatically return you to the start to repeat the procedure.

1. Set up the Function Generator as follows:
   a. Mode: EXT
   b. Signal: Square Wave

2. Perform Linear AM calibration as follows:
   a. At the **$** prompt on the PC screen, type: **`calterm 112`** and press <ENTER>.
   b. Set the function generator to output 0.00 volts. When done, press any key on the keyboard to continue calibration.
   c. Now, set the function generator to output ±0.50 volts. Use the COMPL button on the function generator to toggle the output between +0.50 volts and –0.50 volts.
   d. On the computer keyboard, use 1, 2 or 3 to increment and 8, 9 and 0 to decrement the value of the DAC's setting to obtain a 9.54 dB difference in the power meter's reading when the function generator's output is toggled.

e. When the DAC has been adjusted, press **Q** on the keyboard to exit the program. (If the instrument has a Down Converter installed, you will be returned to the start of the program to perform this calibration for frequencies of >2 GHz.)

When the DAC has been completely adjusted, the program will exit to the **$** prompt.

e. Record step completion on the Test Record.

3. Perform Log AM calibration as follows:

a. At the **$** prompt, type: **calterm 113** and press <ENTER>.

b. Set the function generator for a ±0.20 volt output. Use the COMPL button to toggle the output between –0.20 volts and +0.20 volts.

c. On the computer keyboard, use 1, 2, or 3 to increment and 8, 9, and 0 to decrement the value of the DAC's setting to obtain a 10.00 dB difference in the power meter's reading when the function generator's output is toggled.

d. When the DAC has been adjusted, press **Q** on the keyboard to exit the program. (If the instrument has a Down Converter installed, you will be returned to the start of the program to perform this calibration for frequencies of >2 GHz.)

When the DAC has been completely adjusted, the program will exit to the **$** prompt.

e. Record step completion on the Test Record.

4. Perform AM Meter calibration as follows:

a. At the **$** prompt, type: **calterm 147** and press <ENTER>.

b. Set up the Function Generator for a 1 kHz sinewave with an output level of 0.354 volts RMS (1 volt peak to peak). When done, press any key on the keyboard to continue calibration.

The **$** prompt will appear on the screen when the calibration is complete.

c. Record step completion on the Test Record.

NOTE

To save the calibration data after completing any calibration step, type: **calterm 787** and press <ENTER>.

CAUTION

When saving calibration data, turning off the instrument before the **$** prompt returns to the screen can cause all stored data to be lost.

5. Store the calibration data as follows:
   a. At the **$** prompt, type: **`calterm 787`** and press <ENTER>. (The **$** prompt will appear on the screen when the calibration data has been stored.)
   b. Record step completion on the Test Record.

4-13 FM CALIBRATION (691XXA ONLY)

This procedure provides the steps necessary to perform FM calibration. This consists of calibrating the FM Meter circuit and the FM Gain Control DAC. The FM Gain Control DAC is calibrated for input sensitivities in both narrow and wide FM modes.

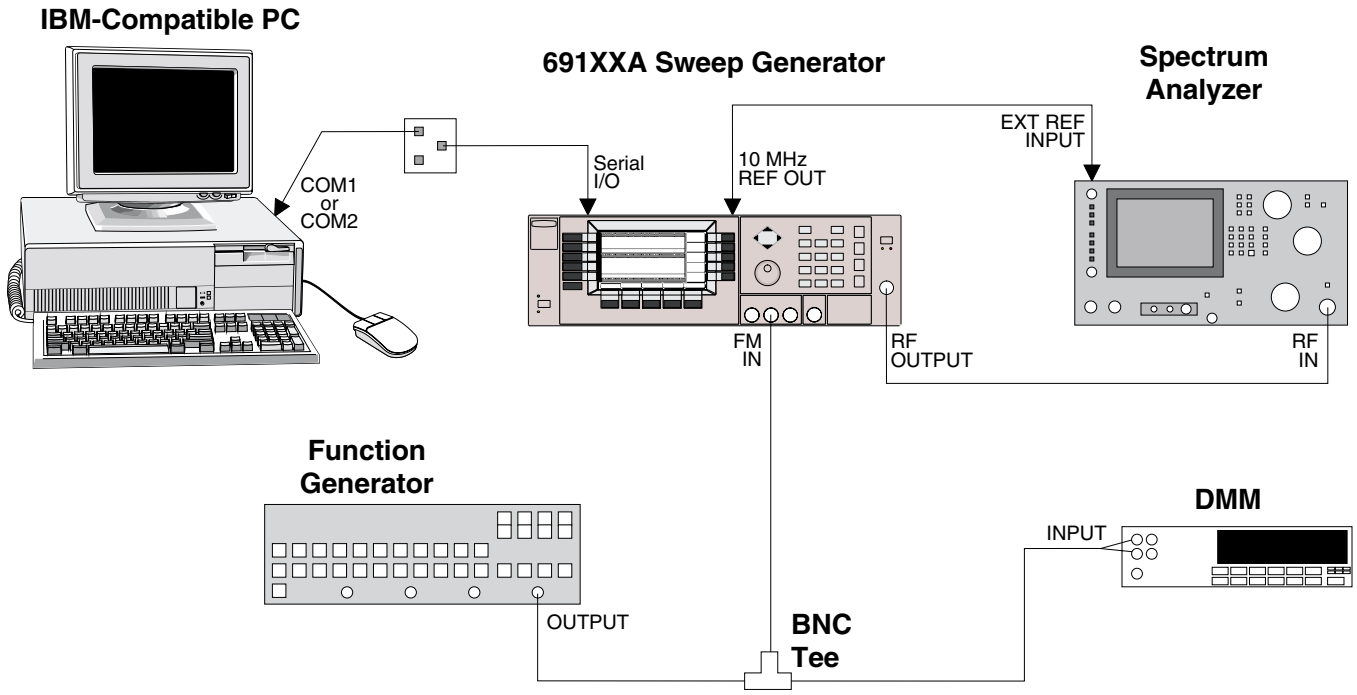


Figure 4-10. *Equipment Setup for FM Calibration*

Equipment Setup

Connect the equipment, shown in Figure 4-10, as follows:

1. Interface the PC to the 691XXA by performing the initial setup procedure, pages 4-7 to 4-12.
2. Connect the 691XXA rear panel 10 MHz REF OUT to the Spectrum Analyzer External Reference input.
3. Connect the Function Generator Output to the BNC tee. Connect one leg of the tee to the 691XXA front panel FM IN. Connect the other leg of the tee to the DMM input.
4. Connect the 691XXA RF OUTPUT to the Spectrum Analyzer RF Input.

NOTE

Before beginning this calibration procedure, always let the 691XXA warm up for a minimum of one hour.

FM Calibration Procedure

The following steps in the procedure lets you calibrate the (1) FM Meter circuit, (2) FM Variable Gain Linearity, (3) FM Narrow and Wide Mode Sensitivity, and (4) FM Rear Panel Input Gain, and store the results in non-volatile memory (EEPROM) on the A17 CPU PCB.

NOTE

To ensure accurate calibration, each step of this procedure must be performed in sequence.

1. Perform FM Meter calibration as follows:
   a. At the **$** prompt on the PC screen, type: **`calterm 123`** and press <ENTER>.
   b. Set up the Function Generator for a 100 kHz sinewave with an output level of 0.707 volts RMS (2 volts peak-to-peak). Use a frequency counter to verify the output frequency of your function generator is set to ±1%. When done, press any key on the keyboard to continue calibration.

      The **$** prompt will appear on the screen when the calibration is complete.
   c. Record step completion on the Test Record.

NOTE

To save the calibration data after completing any calibration step, type: **`calterm 787`** and press <ENTER>.

2. Perform FM Variable Gain Linearity calibration as follows:
   a. At the **$** prompt on the PC screen, type: **`calterm 148`** and press <ENTER>.
   b. Set up the Function Generator for a +1.00 Vdc output. When done, press any key on the keyboard to continue calibration.

      The **$** prompt will appear on the screen when the calibration is complete.
   c. Record step completion on the Test Record.

3. FM Wide Mode Sensitivity calibration is accomplished by adjusting the FM Gain Control DAC to obtain 200 MHz and 20 MHz FM deviations at frequencies of 5 GHz and 15 GHz. Modulating signal inputs are from the external Function Generator.

   Perform the calibration as follows:

   a. At the **$** prompt, type: **`calterm 124`** and press <ENTER>.

   b. Set up the Function Generator for a 0.4 Hz square wave with an output level of 2 volts peak to peak.

   c. On the Spectrum Analyzer, set the Span/Div to 50 MHz per division.

   d. On the computer keyboard, use the `, 1, 2, and 3 keys to increment and the 7, 8, 9, and 0 keys to decrement the value of the DAC's setting. Start calibration by pressing the ` key.

   e. While observing the Spectrum Analyzer display, adjust the value of the DAC's setting to obtain a 200 MHz peak to peak deviation. This is the coarse adjustment.

   f. On the Spectrum Analyzer, set the Span/Div to 5 MHz per division and adjust the center frequency control to position the low carrier at the center of the display. Note the frequency reading.

   g. Now, adjust the center frequency control to position the high carrier at the center of the display. Note the frequency reading.

   h. The difference between these two frequencies is the actual peak-to-peak frequency deviation. It should be 200 MHz ±8 MHz. If not, fine adjust the value of the DAC's setting to obtain this deviation.

   i. When finished setting the DAC, press **Q** on the keyboard to go to the next calibration step (adjusting the DAC to obtain 20 MHz deviation).

   j. Start calibration by pressing the **1** key.

   k. While observing the Spectrum Analyzer display, adjust the value of the DAC's setting to obtain a 20 MHz peak to peak deviation. This is the coarse adjustment.

l. On the Spectrum Analyzer, set the Span/Div to 1 MHz per division and adjust the center fre- to-peak frequency deviation. It should be 20 MHz ±0.8 MHz. If not, fine adjust the value of the DAC's setting to obtain this deviation.

o. When finished setting the DAC, press **Q** on the keyboard to go to the next calibration step (adjusting the DAC to obtain 200 MHz deviation at 15 GHz).

When the DAC has been completely adjusted, the program will exit to the **$** prompt.

p. Record step completion on the Test Record.

4. FM Narrow Mode Sensitivity calibration is accomplished by adjusting the FM Gain Control DAC to reduce the carrier level as low as possible at frequencies of 5 GHz and 15 GHz. Modulating signal inputs are from the external Function Generator.

Perform the calibration as follows:

a. At the **$** prompt, type: **`calterm 125`** and press <ENTER>.

b. Set up the Function Generator for a 99.8 kHz sine wave with an output level of 0.707 volts RMS (2 volts peak to peak). Use a frequency counter to verify the output frequency of your function generator is set to ±1%.

c. On the Spectrum Analyzer, set the Span/Div to 50 kHz per division.

d. On the computer keyboard, use the `, 1, 2, and 3 keys to increment and the 7, 8, 9, and 0 keys to decrement the value of the DAC's setting. Start calibration by pressing an increment key.

e. While observing the first Bessel null (Figure 4-11) on the Spectrum Analyzer display, adjust the value of the DAC's setting to reduce the carrier level as low as possible.

f. When finished setting the DAC, press **Q** on the keyboard to go to the next calibration step.

When the DAC has been completely adjusted, the program will exit to the **$** prompt.

g. Record step completion on the Test Record.

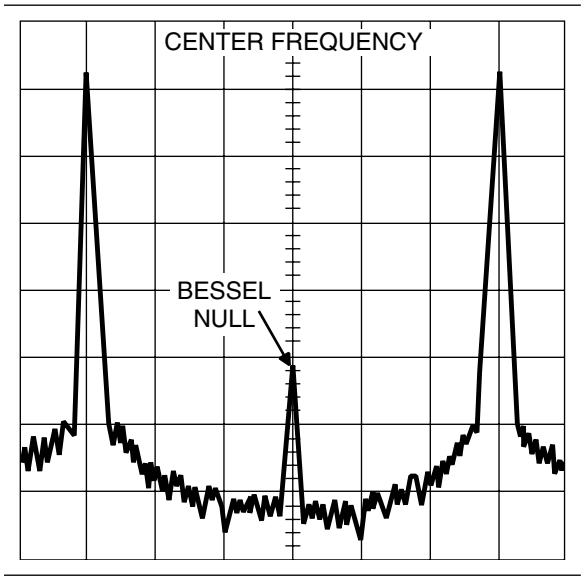


Figure 4-11. *Typical Spectrum Analyzer Display of Bessel Null on FM Waveform*

NOTE

You may need to adjust the RBW setting on the Spectrum Analyzer in order to see the >–40 dBc null.

5. The FM Rear Panel Input Gain is calibrated to balance the FM Narrow Mode Sensitivity obtained when the same external modulating signal is applied to either the front panel or rear panel FM input. Perform the calibration as follows:
   a. On the 691XXA, disconnect the coaxial cable from the front panel FM IN connector and connect it to the rear panel FM IN connector.
   b. At the **$** prompt, type: **calterm 149** and press <ENTER>.
   c. Set up the Function Generator for a 99.8 kHz sine wave with an output level of 0.707 volts RMS (2 volts peak to peak). Use a frequency counter to verify the output frequency of your function generator is set to ±1%.
   d. On the Spectrum Analyzer, set the Span/Div to 50 kHz per division.
   e. On the computer keyboard, use the `, 1, 2, and 3 keys to increment and the 7, 8, 9, and 0 keys to decrement the value of the DAC's setting. Start calibration by pressing an increment key.
   f. While observing the first Bessel null (Figure 4-11) on the Spectrum Analyzer display, adjust the value of the DAC's setting to reduce the carrier level as low as possible.
   f. When finished setting the DAC, press **Q** on the keyboard to exit the calibration routine.
   g. Record step completion on the Test Record.

CAUTION

When saving calibration data, turning off the instrument before the **$** prompt returns to the screen can cause all stored data to be lost.

6. Store the calibration data as follows:
   a. At the **$** prompt, type: **calterm 787** and press <ENTER>. (The **$** prompt will appear on the screen when the calibration data has been stored.)
   b. Record step completion on the Test Record.

Chapter 5
Troubleshooting

Table of Contents

The majority of the troubleshooting procedures presented in this chapter require the removal of the instrument covers to gain access to test points on printed circuit boards and other subassemblies.

WARNING

Hazardous voltages are present inside the 690XXA/691XXA whenever ac line power is connected. Turn off the instrument and remove the line cord before removing any covers or panels. Troubleshooting or repair procedures should only be performed by service personnel who are fully aware of the potential hazards.

CAUTION

Many subassemblies in the instrument contain static-sensitive components. Improper handling of these subassemblies may result in damage to the components. ***Always*** observe the static-sensitive component handling precautions described in Chapter 1, Figure 1-4.

Chapter 5
Troubleshooting

5-1 INTRODUCTION

This chapter provides information for troubleshooting 690XXA/691XXA malfunctions. The troubleshooting procedures presented in this chapter support fault isolation to a replaceable subassembly or RF component. (Remove and replace procedures for the subassemblies and RF components are found in Chapter 6.)

5-2 RECOMMENDED TEST EQUIPMENT

The recommended test equipment for the troubleshooting procedures presented in this chapter is listed in Chapter 1, Table 1-2 (page 1-12).

5-3 ERROR AND WARNING/STATUS MESSAGES

During normal operation, the 690XXA/691XXA generates error messages to indicate internal malfunctions, abnormal instrument operations, or invalid signal inputs or data entries. It also displays warning messages to alert the operator to conditions that could result in inaccurate 690XXA/691XXA output. In addition, status messages are displayed to remind the operator of current menu selections or settings.

Self-Test Error Messages

The 690XXA/691XXA firmware includes internal diagnostics that self-test the instrument. These self-test diagnostics perform a brief go/no-go test of most of the instrument PCBs and other internal assemblies.

You can perform an instrument self-test at any time during normal operation by pressing **SYSTEM** and then the System Menu soft-key Selftest.

If the 690XXA/691XXA fails self-test, an error message(s) is displayed on the front panel data display. These error messages describe the malfunction and, in most cases, provide an indication of what has failed. Table 5-1 is a summary listing of the self-test error messages. Included for each is a reference to the troubleshooting table that provides a description of the probable cause(s) and a procedure for identifying the failed component or assembly.

Table 5-1. *Self-Test Error Messages (1 of 3)*

Error Message	Troubleshooting Table	Page Number
Error 100 DVM Ground Offset Failed	5-5	5-15
Error 101 DVM Positive 10V Reference	5-5	5-15
Error 102 DVM Negative 10V Reference	5-5	5-15
Error 105 Power Supply Voltage(s) out of Regulation	5-6	5-16
Error 106 Power Supply not Locked	5-6	5-25
Error 107 Sweep Time Check Failed	5-16	5-33
Error 108 Crystal Oven Cold	5-8	5-26
Error 109 The 100MHz Reference is not Locked to the External Reference	5-8	5-26
Error 110 The 100MHz Reference is not Locked to the High Stability 10MHz Crystal Oscillator	5-8	5-27
Error 111 Fine Loop Osc Failed	5-9	5-28
Error 112 Coarse Loop B Osc Failed	5-11	5-29
Error 113 Yig Loop Osc Failed	5-13	5-30
Error 114 Down Converter LO not Locked	5-14	5-31
Error 115 Not Locked Indicator Failed	5-13	5-31
Error 116 FM Loop Gain Check Failed	5-15	5-32
Error 117 Linearizer Check Failed	5-16	5-33
Error 118 Switchpoint DAC Failed	5-16	5-33
Error 119 Center Frequency Circuits Failed	5-16	5-33

Table 5-1. *Self-Test Error Messages (2 of 3)*

Error Message	Troubleshooting Table	Page Number
Error 120 Delta-F Circuits Failed	5-16	5-33
Error 121 Unleveled Indicator Failed	5-17	5-34
Error 122 Level Reference Failed	5-17	5-34
Error 123 Detector Log Amp Failed	5-17	5-34
Error 124 Full Band Unlocked and Unleveled	5-18	5-36
Error 125 8.4 – 20 GHz Unlocked and Unleveled	5-18	5-36
Error 126 2 – 8.4 GHz Unlocked and Unleveled	5-18	5-36
Error 127 Detector Input Circuit Failed	5-17	5-34
Error 128 .01 – 2 GHz Unleveled	5-20	5-38
Error 129 Switched Filter or Level Detector Failed	5-20	5-41
Error 130 2 – 3.3 GH Switched Filter	5-20	5-44
Error 131 3.3 – 5.5 GH Switched Filter	5-20	5-44
Error 132 5.5 – 8.4 GH Switched Filter	5-20	5-44
Error 133 8.4 – 13.25 GH Switched Filter	5-20	5-44
Error 134 13.25 – 20 GH Switched Filter	5-20	5-44
Error 135 Modulator or Driver Failed	5-20	5-45
Error 142 Sample and Hold Circuit Failed	5-17	5-34
Error 143 Slope DAC Failed	5-17	5-35

Table 5-1. *Self-Test Error Messages (3 of 3)*

Error Message	Troubleshooting Table	Page Number
Error 144 RF was Off when Selftest started. Some tests were not performed.	5-24	5-48
Error 149 Coarse Loop C Osc Failed	5-11	5-29
690XXA/691XXA Models with SDM		
Error 138 SDM Unit or Driver Failed	5-22	5-46
Error 139 32 – 40 GHz SDM Section Failed	5-22	5-47
Error 140 25 – 32 GHz SDM Section Failed	5-22	5-47
Error 141 20 – 25 GHz SDM Section Failed	5-22	5-47

Normal Operation Error and Warning/ Status Messages

When an abnormal condition is detected during operation, the 690XXA/691XXA displays an error message to indicate that the output is abnormal or that a signal input or data entry is invalid. It also displays warning messages to alert the operator to conditions that could cause an inaccurate instrument output. Status messages to remind the operator of current menu selections or settings are also generated.

Table 5-2 is a summary list of possible error messages that can be displayed during normal operations. Table 5-3 is a summary list of possible warning/status messages.

Table 5-2. *Possible Error Messages during Normal Operations*

Error Message	Description
ERROR	Displayed (on the frequency mode title bar) when (1) the output frequency is not phase-locked or (2) an invalid entry causes a frequency range error.
LOCK ERROR	Displayed (in the frequency parameters area) when the output frequency is not phase-locked. The frequency accuracy and stability of the RF output is greatly reduced. Normally caused by an internal component failure. Run self-test to verify malfunction.
RANGE	Displayed (in the frequency parameters area) when (1) the analog sweep start frequency entered is greater than the stop frequency (691XXA models only), (2) the dF value entered results in a sweep outside the range of the instrument, (3) the step size value entered is greater than the sweep range, or (4) the number of steps entered results in a step size of less than 1 kHz (0.1 Hz with Option 11) or 0.1 dB. Entering valid values usually clears the error.
ERR	*(691XXA models only)* Displayed (in the modulation status area) when either the external AM modulating signal or the external FM modulating signal exceeds the input voltage range. In addition, the message "**Reduce AM (FM) Input Level**" appears at the bottom of the AM (FM) status display. AM (FM) will be turned off until the modulating signal is in the input voltage range.
SLAVE	Displayed (in the frequency parameters area of the Master 68XXXB/69XXXA) during master-slave operation when the slave frequency offset value entered results in a CW frequency or frequency sweep outside the range of the slave 68XXXB/69XXXA. Entering a valid offset value clears the error.

Table 5-3. *Possible Warning/Status Messages during Normal Operation*

Warning/Status Message	Description
OVN COLD	This warning message indicates that the 100 MHz Crystal oven (or the 10 MHz Crystal oven if Option 16 is installed) has not reached operating temperature. Normally displayed during a cold start of the instrument. If the message is displayed during normal operation, it could indicate a malfunction. Run self-test to verify.
UNLEVELED	Displayed when the RF output goes unleveled. Normally caused by exceeding the specified leveled-power rating. Reducing the power level usually clears the warning message. (*691XXA models only*) If the warning message is displayed only when AM is selected ON, the modulating signal may be driving the RF output unleveled. Reducing the modulating signal or adjusting the power level usually clears the warning.
UNLOCKED	*(691XXA models only)* When FM is selected ON or Unlocked Narrow FM or Unlocked Wide FM is selected ON, this warning message appears indicating that the instrument is not phase-locked during this FM mode of operation.
EXT REF	This status message indicates that an external 10 MHz signal is being used as the reference signal for the 690XXA/691XXA.
OFFSET	This status message indicates that a constant (offset) has been applied to the displayed power level.
SLOPE	This status message indicates that a power slope correction has been applied to the ALC.
USER 1...5	This status message indicates that a user level flatness correction power-offset table has been applied to the ALC.
SS MODE	*(691XXA models only)* This status message indicates that the 691XXA has been placed in a source lock mode for operation with a 360B Vector Network Analyzer.

5-4 MALFUNCTIONS NOT DISPLAYING AN ERROR MESSAGE

The 690XXA/691XXA must be operating to run self-test. Therefore, malfunctions that cause the instrument to be non-operational do not produce error messages. These problems generally are a failure of the 690XXA/691XXA to power up properly. Table 5-4, beginning on page 5-11, provides troubleshooting procedures for these malfunctions.

In those 690XXA/691XXA models that produce RF outputs of >40 GHz, malfunctions related to quadrupling the source signal do not generate error messages. Troubleshooting procedures for these malfunctions are included in Table 5-4.

5-5 TROUBLESHOOTING TABLES

Tables 5-4 through 5-24, beginning on page 5-11, provide procedures for isolating malfunctions to a replaceable subassembly or RF component. In those cases where any of several subassemblies or RF components could have caused the problem, subassembly/RF component replacement is indicated. The recommended replacement order is to replace first the subassemblies/RF components that are most likely to have failed.

Figure 5-1, on the following page, shows the location of the 690XXA/691XXA connectors and test points that are called out in the troubleshooting procedures of Tables 5-4 through 5-24.

CAUTION

Never remove or replace a subassembly or RF component with power applied. Serious damage to the instrument may occur.

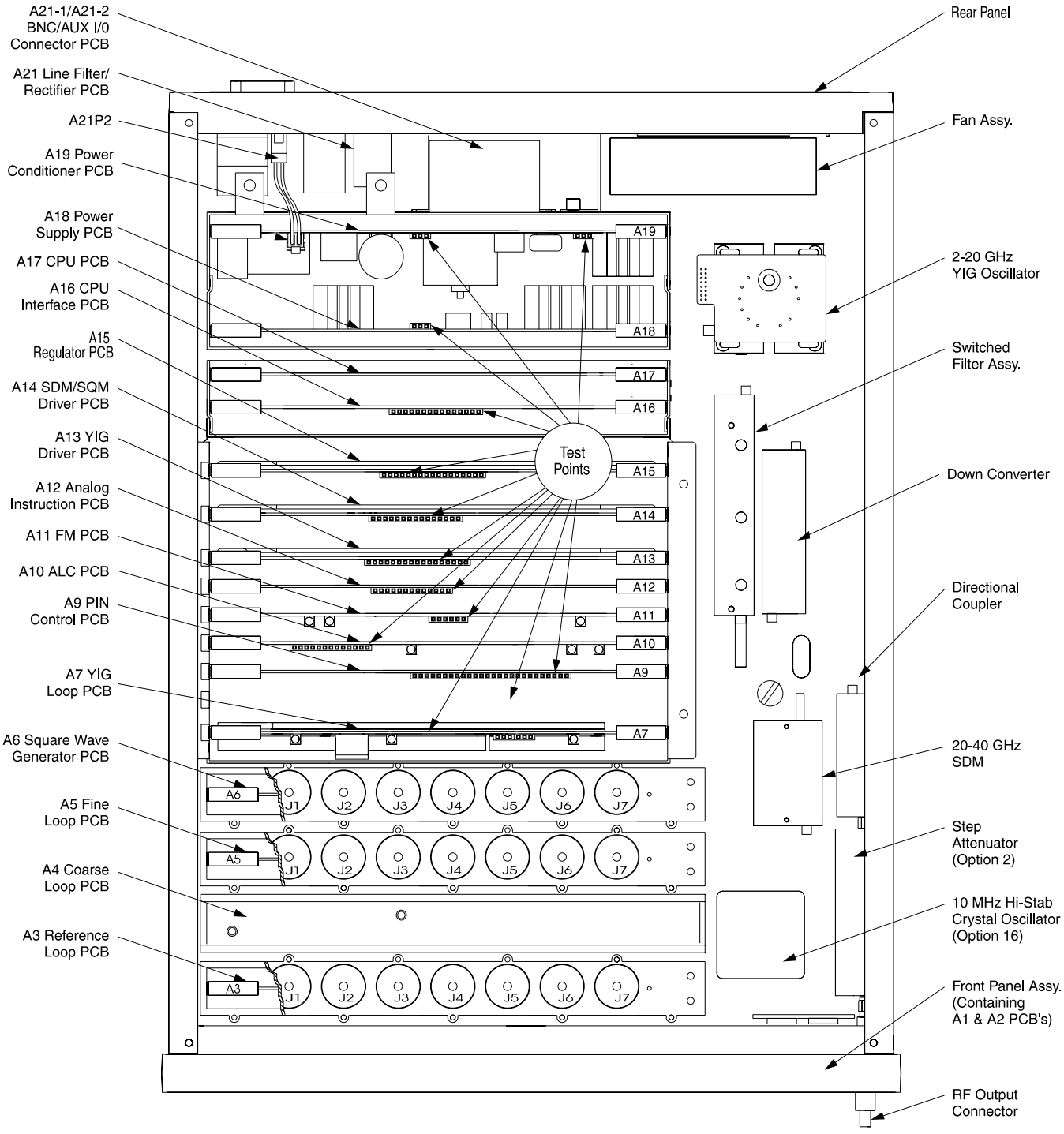


Figure 5-1. *Top View of the 690XXA/691XXA Showing Connector and Test Point Locations*

Table 5-4. *Malfunctions Not Displaying an Error Message (1 of 4)*

690XXA/691XXA Will Not Turn On (OPERATE light is OFF)

Normal Operation: When the 690XXA/691XXA is connected to the power source, the OPERATE light should illuminate and the instrument should power up.

Step 1. Disconnect the 690XXA/691XXA from the power source, then check the line fuse on the rear panel.

- ❑ If the line fuse is good, go to step 2.
- ❑ If the line fuse is defective, replace but do **not** apply power. Go to step 2.

Step 2. Remove the 690XXA/691XXA top cover and the cover over the A18 and A19 PCBs.

Step 3. After connecting the negative lead of a digital multimeter (DMM) to A19TP5 and the positive lead to A19TP6, connect the 690XXA/691XXA to the power source and check for a 330 volt reading on the DMM.

- ❑ If the voltage is correct, go to step 4.
- ❑ If the voltage is incorrect or the line fuse blows, replace the A21 Line Filter/Rectifier PCB (located on the rear panel).

Step 4. Connect the negative lead of the DMM to A19TP3 and the positive lead to A19TP2, then check for a +28 ±2 volt reading on the DMM.

- ❑ If the voltage is correct, go to step 5.
- ❑ If the voltage is incorrect or the line fuse blows, replace the A19 PCB.

Step 5. Connect the negative lead of the DMM to A15TP1 and the positive lead to A15TP14, then check for a +23.33 ±0.5 volts reading on the DMM.

- ❑ If the voltage is correct, the Front Panel assembly or the cable between Motherboard connector A20J22 and the Front Panel assembly may be defective.
- ❑ If the voltage is incorrect, the +24V standby power supply may be loaded down by (1) a shorted oven heater for the 100 MHz reference oscillator located on the A3 PCB, (2) a shorted heater for the optional 10 MHz high stability time base (if installed), or (3) a defective Front Panel assembly.

Table 5-4. *Malfunctions Not Displaying an Error Message (2 of 4)*

690XXA/691XXA Will Not Turn On (OPERATE light is ON)

Normal Operation: When the 690XXA/691XXA is connected to the power source, the OPERATE light should illuminate and the instrument should power up.

Step 1. Remove the 690XXA/691XXA top cover and the cover over the A18 and A19 PCBs.

Step 2. Connect the negative lead of the DMM to A18TP1 and the positive lead to A18TP3.

Step 3. Check for a +23.3 ±0.5 volt reading on the DMM.

- ❑ If the voltage is correct, go to step 4.
- ❑ If the voltage is incorrect or missing, the Front Panel assembly or the cable between Motherboard connector A20J22 and the Front Panel assembly may be defective.

Step 4. Press the front panel RF OUTPUT ON/OFF button. Do the yellow and red LEDs toggle?

- ❑ If yes, the malfunction may be caused by a failed front panel circuit. Replace the Front Panel assembly.
- ❑ If the LEDs do not toggle or if both LEDs are lit, the problem may be caused by a malfunction on the A17 CPU PCB.

Table 5-4. *Malfunctions Not Displaying an Error Message (3 of 4)*

Output Power Related Problems (>40 GHz) 690XXA/691XXA Models with SQM

Description: The CW/sweep generator does not display any error message during self-test; however, there is no or low RF output above 40 GHz.

Step 1. Set up the 690XXA/691XXA as follows:

a. 690XXA Setup:
CW/SWEEP SELECT: Step
F1: 40.0 GHz
F2: 50.0, 60.0, or 65.0 GHz (Model dependent)
Number of Steps: 400
L1: –2.0 dBm

691XXA Setup:
CW/SWEEP SELECT: Analog
F1: 40.0 GHz
F2: 50.0, 60.0, or 65.0 GHz (Model dependent)
Sweep Time: 0.100 Sec
L1: –2.0 dBm

Step 2. Connect the X input of an oscilloscope to the 690XXA/691XXA rear panel HORIZ OUT connector.

Step 3. Using the oscilloscope, check the following voltages:

a. For models having a high end frequency of 50 GHz, check the SQM bias voltages at A14TP5 and A14TP7. The bias voltage at A14TP5 should be +10 volts; the bias voltage at A14TP7 should be –5 volts.

For models having a high end frequency of 60 or 65 GHz, check for a +12 volts SQM bias voltage at A14TP6.

b. For all models, check for a –2 volt PIN switch drive voltage at A9TP22.

- ❑ If the SQM bias and the PIN switch drive voltages are correct, go to step 4.
- ❑ If the SQM bias voltage(s) is not correct, replace the A14 PCB.
- ❑ If the PIN switch drive voltage is not correct, replace the A9 PCB.

Table 5-4. *Malfunctions Not Displaying an Error Message (4 of 4)*

Step 4. Connect a 562 Scalar Network Analyzer to the 690XXA/691XXA as follows:

a. Connect the 690XXA/691XXA AUX I/O to the 562 AUX I/O.

b. Connect the 562 DEDICATED GPIB to the 690XXA/691XXA IEEE-488 GPIB.

c. Connect the RF Detector to the 562 Channel A Input.

Step 5. Set up the 562 Scalar Network Analyzer as follows:

a. Press SYSTEM MENU display.

b. From System Menu display, select RESET.

c. Press CHANNEL 2 DISPLAY: OFF.

d. Press CHANNEL 1 DISPLAY: ON.

e. Press CHANNEL 1 Menu key.

f. From the Channel 1 Menu display, select POWER.

Step 6. Using the scalar network analyzer, measure the RF output at J4 of the switched filter assembly. The amplitude of the RF signal should be >+18 dBm throughout the full sweep.

- If the amplitude of the RF signal is correct, replace the SQM.
- If there is no RF signal or if the amplitude of the RF signal is low, replace the switched filter assembly.

Table 5-5. *Error Messages 100. 101, and 102*

Internal DVM Tests

Error 100 DVM Ground Offset Failed, *or*
Error 101 DVM Positive 10V Reference, *or*
Error 102 DVM Negative 10V Reference

Description: The DVM circuitry, located on the A16 CPU Interface PCB, is calibrated using the ±10 volts from the reference supplies on the A12 Analog Instruction PCB. The error messages indicate a calibration-related problem or a defective ±10 volt reference.

Step 1. Perform a manual pre-calibration. (Refer to chapter 4 for the calibration procedure.)

Step 2. Run self-test.

- ❑ If no error message is displayed, the problem is cleared.
- ❑ If any of the error messages, 100, 101, and 102, are displayed, go to step 3.

Step 3. Connect the negative lead of the digital multimeter to A12TP1.

Step 4. Measure the ±10V reference voltages at A12TP4 and A12TP8. A12TP4 should be –10V ±0.036V; A12TP8 should be +10V ±0.036V.

- ❑ If the ±10V reference voltages are correct, go to step 5.
- ❑ If incorrect, replace the A12 PCB.

NOTE

Even if the ±10V reference voltages are correct, there could still be a malfunction of the DVM multiplexer on the A12 PCB or the DVM circuitry on the A16 CPU Interface PCB.

Step 5. Replace the A12 PCB and run self-test again.

- ❑ If no error message is displayed, the problem is cleared.
- ❑ If any of the error messages, 100, 101, and 102, are displayed, go to step 6.

Step 6. Replace the A16 PCB, then run self-test.

- ❑ If no error message is displayed, the problem is cleared.
- ❑ If any of the error messages, 100, 101, and 102, are displayed, contact your local ANRITSU service center for assistance.

Table 5-6. *Error Messages 105 and 106 (1 of 10)*

Power Supply Tests

WARNING

Voltages hazardous to life are present throughout the power supply circuits, *even when the front panel* LINE *switch is in the* STANDBY *postion*. When performing maintenance, use utmost care to avoid electrical shock.

Error 105 Power Supply Voltage(s) out of Regulation.

Description: The out of regulation circuit, located on the A15 Regulator PCB, monitors all of the regulated power supply outputs. This error message indicates that one of more of the voltages from the power supply, with the exception of the 5 volt supply, is out of regulation. If the 5 volt supply is faulty, the 690XXA/691XXA will not operate.

Step 1. Measure the regulated voltages at the test points shown in Table 5-7.

- ❑ If incorrect for a supply, go to the referenced step.
- ❑ If incorrect for several supplies, go to step 2.
- ❑ If all voltages are correct, go to step 3.

Table 5-7. *Regulated Power Supply Voltages*

Regulated Voltage	Measurement Point	Reference Point	Value	Refer to Step
+15VG	A15 TP3	A15 TP1	+15V ±0.75V	4
–15VG	A15 TP9	A15 TP1	–15V ±0.75V	4
+15VA	A15 TP2	A15 TP1	+15 ±0.75V	5
–15VA	A15 TP7	A15 TP1	–15V ±0.75V	5
+15VLP	A15 TP12	A15 TP1	+15V ±0.75V	6
–15VLP	A15 TP13	A15 TP1	–15V ±0.75V	6
+15VFM	A15 TP8	A15 TP1	+15V ±0.75V	7
–15VFM	A15 TP11	A15 TP1	–15V ±0.75V	7
–18VT	A15 TP10	A15 TP1	–18V ±0.36V	8
–43VT	A15 TP15	A15 TP1	–43V ±0.9V	9
+24VH	A15 TP6	A15 TP1	+24.32V ± .5V	10

Table 5-6. *Error Messages 105 and 106 (2 of 10)*

Step 2. Perform the following procedure to isolate malfunctions when the voltages from several regulated supplies are incorrect.

a. Place the LINE switch to STANDBY.

b. Replace the A15 PCB assembly.

c. Place the LINE switch to OPERATE and measure the regulated voltages per Table 5-7.

- ❑ If the voltages are correct, the problem is cleared.
- ❑ If the voltages are incorrect, go to step d.

d. Place the LINE switch to STANDBY.

e. Replace the A18 PCB.

f. Place the LINE switch to OPERATE and measure the regulated voltages per Table 5-7.

- ❑ If the voltages are correct, the problem is cleared.
- ❑ If the voltages are still incorrect, contact your local ANRITSU service center for assistance.

Step 3. Run self-test again.

- ❑ If no error message is displayed, the problem is cleared.
- ❑ If error 105 displays again, contact your local ANRITSU service center for assistance.

Table 5-6. *Error Messages 105 and 106 (3 of 10)*

±15VG Supply Problems

This supply provides ±15 volts to the YIG Driver; SDM, SQM Driver; and CPU I/O circuits and the YIG-tuned Oscillator, Switched Filter, and Down Converter assemblies.

Step 4. Perform the following procedure to isolate malfunctions to the ±15VG supply and outlying load circuits.

a. Place the LINE switch to STANDBY.

b. Replace the A15 PCB assembly.

c. Place the LINE switch to OPERATE and measure the ±15VG voltages per Table 5-7.

- ❑ If the voltages are correct, the problem is cleared.
- ❑ If the voltages are incorrect, go to step d.

d. Place the LINE switch to STANDBY.

e. Remove the A13, A14, and A16 PCBs as applicable for your model.

f. Place the LINE switch to OPERATE and measure the ±15VG voltages.

- ❑ If the voltages are correct, go to step j.
- ❑ If the voltages are still incorrect, go to step g.

g. Place the LINE switch to STANDBY.

h. Remove the YIG-tuned oscillator, switched filter, and down converter assemblies.

i. Place the LINE switch to OPERATE and measure the ±15VG voltages.

- ❑ If the voltages are correct, go to step j.
- ❑ If the voltages are still incorrect, contact your local ANRITSU service center for assistance.

j. Place the LINE switch to STANDBY, then install one of the removed PCBs/assemblies.

k. Place the LINE switch to OPERATE and measure the ±15VG voltages.

l. Continue steps j and k until the faulty PCB/assembly is located.

Table 5-6. *Error Messages 105 and 106 (4 of 10)*

±15VA Supply Problems

This supply provides ±15 volts to the PIN Control, ALC, and Analog Instruction circuits.

Step 5. Perform the following procedure to isolate malfunctions to the ±15VA supply and outlying load circuits.

a. Place the LINE switch to STANDBY.

b. Replace the A15 PCB assembly.

c. Place the LINE switch to OPERATE and measure the ±15VA voltages per Table 5-7.

- ❑ If the voltages are correct, the problem is cleared.
- ❑ If the voltages are incorrect, go to step d.

d. Place the LINE switch to STANDBY.

e. Remove the A9, A10, and A12 PCBs.

f. Place the LINE switch to OPERATE and measure the ±15VA voltages.

- ❑ If the voltages are correct, go to step g.
- ❑ If the voltages are still incorrect, contact your local ANRITSU service center for assistance.

g. Place the LINE switch to STANDBY, then install one of the removed PCBs/assemblies.

h. Place the LINE switch to OPERATE and measure the ±15VA voltages.

i. Continue steps g and h until the faulty PCB/assembly is located.

Table 5-6. *Error Messages 105 and 106 (5 of 10)*

±15VLP Supply Problems

This supply provides ±15 volts to the Reference, Coarse, Fine, and YIG Phase-Lock Loop circuits.

Step 6. Perform the following procedure to isolate malfunctions to the ±15VLP supply and outlying load circuits.

a. Place the LINE switch to STANDBY.

b. Replace the A15 PCB assembly.

c. Place the LINE switch to OPERATE and measure the ±15VLP voltages per Table 5-7.

- ❑ If the voltages are correct, the problem is cleared.
- ❑ If the voltages are incorrect, go to step d.

d. Place the LINE switch to STANDBY.

e. Remove the A3, A4, A5, and A7 PCBs.

f. Place the LINE switch to OPERATE and measure the ±15VLP voltages.

- ❑ If the voltages are correct, go to step g.
- ❑ If the voltages are still incorrect, contact your local ANRITSU service center for assistance.

g. Place the LINE switch to STANDBY, then install one of the removed PCBs/assemblies.

h. Place the LINE switch to OPERATE and measure the ±15VLP voltages.

i. Continue steps g and h until the faulty PCB/assembly is located.

Table 5-6. *Error Messages 105 and 106 (6 of 10)*

±15VFM Supply Problems

This supply provides ±15 volts to the FM portion of the YIG Driver circuits.

Step 7. Perform the following procedure to isolate malfunctions to the ±15VFM supply and its outlying load circuit.

a. Place the LINE switch to STANDBY.

b. Replace the A15 PCB assembly.

c. Place the LINE switch to OPERATE and measure the ±15VFM voltages per Table 5-7.

- ❑ If the voltages are correct, the problem is cleared.
- ❑ If the voltages are incorrect, go to step d.

d. Place the LINE switch to STANDBY.

e. Remove the A13 PCB.

f. Place the LINE switch to OPERATE and measure the ±15VFM voltages.

- ❑ If the voltages are correct, replace the A13 PCB.
- ❑ If the voltages are still incorrect, contact your local ANRITSU service center for assistance.

Table 5-6. *Error Messages 105 and 106 (7 of 10)*

–18VT Supply Problems

This supply provides –18 volts to the front panel LCD contrast circuit and to drive the YIG-tuned oscillator main tuning coil during CW and slow analog sweeps.

Step 8. Perform the following procedure to isolate malfunctions to the –18VT supply and its outlying load circuit.

a. Place the LINE switch to STANDBY.

b. Replace the A15 PCB assembly.

c. Place the LINE switch to OPERATE and measure the –18VT voltage per Table 5-7.

- ❑ If the voltage is correct, the problem is cleared.
- ❑ If the voltage is incorrect, go to step d.

d. Place the LINE switch to STANDBY.

e. Remove the A13 PCB and the YIG-tuned oscillator assembly.

f. Place the LINE switch to OPERATE and measure the –18VT voltage.

- ❑ If the voltage is correct, go to step i.
- ❑ If the voltage is still incorrect, go to step g.

g. Replace the front panel assembly by following the steps in paragraph 6-3 of Chapter 6—Removal and Replacement Procedures.

h. Place the LINE switch to OPERATE and measure the –18VT voltage.

- ❑ If the voltage is correct, the problem is cleared.
- ❑ If the voltage is still incorrect, contact your local ANRITSU service center for assistance.

i. Place the LINE switch to STANDBY.

j. Install the A13 PCB.

k. Place the LINE switch to OPERATE and measure the –18VT voltage.

- ❑ If the voltage is correct, replace the YIG-tuned oscillator assembly.
- ❑ If the voltage is incorrect, replace the A13 PCB.

Table 5-6. *Error Messages 105 and 106 (8 of 10)*

–43VT Supply Problems

This supply provides –43 volts to drive the YIG-tuned oscillator main tuning coil during bandswitching, fast analog sweeps, and digital sweeps.

Step 9. Perform the following procedure to isolate malfunctions to the –43VT supply and its outlying load circuit.

a. Place the LINE switch to STANDBY.

b. Replace the A15 PCB assembly.

c. Place the LINE switch to OPERATE.

d. Set up the 690XXA/691XXA to perform a 2 to 20 GHz step sweep.

e. Measure the –43VT voltage per Table 5-7.

- ❑ If the voltage is correct, the problem is cleared.
- ❑ If the voltage is incorrect, go to step f.

f. Place the LINE switch to STANDBY.

g. Remove the A13 PCB and the YIG-tuned oscillator assembly.

h. Place the LINE switch to OPERATE and measure the –43VT voltage.

- ❑ If the voltage is correct, go to step i.
- ❑ If the voltage is still incorrect, contact your local ANRITSU service center for assistance.

i. Place the LINE switch to STANDBY.

j. Install the A13 PCB.

k. Place the LINE switch to OPERATE and measure the –43VT voltage.

- ❑ If the voltage is correct, replace the YIG-tuned oscillator assembly.
- ❑ If the voltage is incorrect, replace the A13 PCB.

Table 5-6. *Error Messages 105 and 106 (9 of 10)*

+24VH Supply Problems

This supply provides +24 volts for the YIG-tuned oscillator heater, the step attenuator drivers and relay circuit on the A9 PCB, the V/GHz circuit on the A12 PCB, and coarse, fine, and YIG loop circuits. When the 690XXA/691XXA is switched to OPERATE, it also takes over the function of the 24VS supply and supplies +24 volts to the 100 MHz reference oscillator oven heater, the front panel LINE switch circuitry, and the optional 10 MHz high stability time base oven heater.

Step 10. Perform the following procedure to isolate malfunctions to the +24VH supply and outlying load circuits.

a. Place the LINE switch to STANDBY.

b. Replace the A15 PCB assembly.

c. Place the LINE switch to OPERATE and measure the +24VH voltage per Table 5-7.

- ❑ If the voltage is correct, the problem is cleared.
- ❑ If the voltage is incorrect, go to step d.

d. Place the LINE switch to STANDBY.

e. Remove the A4, A5, A7, A9, and A12 PCBs and the YIG-tuned oscillator assembly.

f. Place the LINE switch to OPERATE and measure the +24VH voltage.

- ❑ If the voltage is correct, go to step g.
- ❑ If the voltage is still incorrect, contact your local ANRITSU service center for assistance.

g. Place the LINE switch to STANDBY, then install one of the removed PCBs or the YIG-tuned oscillator assembly.

h. Place the LINE switch to OPERATE and measure the +24VH voltage.

i. Continue steps g and h until the faulty PCB/assembly is located.

Table 5-6. *Error Messages 105 and 106 (10 of 10)*

Power Supply Not Phase-Locked

Error 106 Power Supply not Locked

Description: The switching power supply is not phase locked to the 400 kHz reference signal from the A6 Square Wave Generator PCB.

Step 1. Using an oscilloscope, verify the presence of a 400 kHz TTL square wave at TP4 on the A6 PCB.

- ❑ If present, replace the A18 Power Supply PCB.
- ❑ If not present, go to step 2.

Step 2. Using an oscilloscope, verify the presence of a 10 MHz TTL signal at J4 of the A5 Fine Loop PCB.

- ❑ If present, go to step 3.
- ❑ If not present, go to step 4.

Step 3. Check the cable, W108, that goes between A5J4 and A6J1.

- ❑ If the cable is good, replace the A6 PCB.
- ❑ If the cable has failed, replace it.

Step 4. Using a spectrum analyzer, verify the presence of a +3 dBm ±5 dB, 10 MHz signal at J4 of the A3 Reference Loop PCB.

- ❑ If present, go to step 5.
- ❑ If not present, replace the A3 PCB.

Step 5. Check the cable, W136, that goes between A3J4 and A5J5.

- ❑ If the cable is good, replace the A5 PCB.
- ❑ If the cable has failed, replace it.

Table 5-8. *Error Messages 108, 109 and 110 (1 of 2)*

A3 Reference Loop

Error 108 Crystal Oven Cold

Description: The oven of the 100 MHz crystal oscillator or the Option 16 high-stability 10 MHz crystal oscillator has not reached operating temperature.

Step 1. Allow a 30 minute warm up, then run self-test again.

- ❑ If error 108 is not displayed, the problem is cleared.
- ❑ If error 108 displays and Option 16 is not installed, replace the A3 PCB.
- ❑ If error 108 displays and Option 16 is installed, go to step 2.

Step 2. Disconnect the cable between Motherboard connector A20J4 and the Option 16 crystal oscillator assembly.

Step 3. Run self-test again.

- ❑ If error 108 is not displayed, replace the Option 16 crystal oscillator assembly.
- ❑ If error 108 is still displayed, replace the A3 PCB.

Error 109 The 100MHz Reference is not phase-locked to the External Reference

Description: The reference loop is not phase-locked to the external 10 MHz reference.

Step 1. Using a coaxial cable with BNC connectors, connect the rear panel 10 MHz REF IN connector to the rear panel 10 MHz REF OUT connector.

Step 2. Disconnect the cable, W110, from A3J7.

Step 3. Using an oscilloscope, verify the presence of a 10 MHz signal at the end of the cable. The signal amplitude should be >0.5 volts peak-to-peak (into 50Ω).

- ❑ If present, replace the A3 PCB.
- ❑ If not present, replace the cable W110.

Table 5-8. *Error Messages 108, 109 and 110 (2 of 2)*

Error 110 The 100MHz Reference is not Locked to the High Stability 10MHz Crystal Oscillator

Description: The reference loop is not phase-locked to the Option 16 high stability 10 MHz crystal oscillator.

Step 1. Disconnect the cable from A3J6.

Step 2. Using an oscilloscope, verify the presence of a 10 MHz signal at the end of the cable. The signal amplitude should be ≥1 volt (into 50Ω).

- ❑ If present, replace the A3 PCB.
- ❑ If not present, replace the Option 16 crystal oscillator assembly.

Table 5-9. *Error Message 111*

A5 Fine Loop

Error 111 Fine Loop Osc Failed

Description: One or more of the oscillators within the fine loop is not phase-locked.

Step 1. Disconnect cable W136 at A5J5.

Step 2. Using a spectrum analyzer, verify the presence of a +3 dBm ±5 dB, 10 MHz signal at the end of the cable.

- ❑ If present, go to step 5.
- ❑ If not present, go to step 3.

Step 3. Disconnect cable W136 at A3J4.

Step 4. Using the spectrum analyzer, verify the presence of the +3 dBm, ±5 dB, 10 MHz signal at A3J4.

- ❑ If present, replace the cable W136.
- ❑ If not present, replace the A3 PCB.

Step 5. Reconnect cable W136 to A5J5 and disconnect cable W107 at A5J1.

Step 6. Set up the 690XXA/691XXA to generate the CW frequencies listed in Table 5-10.

Table 5-10. *Fine Loop Frequencies*

690XXA/691XXA CW Frequency	Measured Frequency at A5J1
8.310 GHz	40 MHz
8.309 GHz	31 MHz

Step 7. Using a spectrum analyzer, measure the frequency and amplitude of the signal at A5J1 for each of the CW frequencies generated. In each case, the signal amplitude should be +3 dBm ±3 dB with sidebands at <–65 dBc.

- ❑ If the signals are correct in both frequency and amplitude, go to step 8.
- ❑ If the signals are incorrect, replace the A5 PCB.

Step 8. Reconnect cable W107 to A5J1 and run self-test again.

- ❑ If error 111 is not displayed, the problem is cleared.
- ❑ If error 111 is still displayed, contact your local ANRITSU service center for assistance.

Table 5-11. *Error Messages 112 and 149*

A4 Coarse Loop

Error 112 Coarse Loop B Osc Failed
Error 149 Coarse Loop C Osc Failed

Description: One of the oscillators within the coarse loop is not phase-locked.

Step 1. Disconnect cable W134 at A4J1.

Step 2. Using a spectrum analyzer, verify the presence of a +5 dBm ±6 dB, 100 MHz signal at the end of cable W134.

- ❑ If present, go to step 5.
- ❑ If not present, go to step 3.

Step 3. Disconnect cable W134 at A3J3.

Step 4. Using the spectrum analyzer, verify the presence of the +5 dBm ±6 dB, 100 MHz signal at A3J3.

- ❑ If present, replace cable W134.
- ❑ If not present, replace the A3 PCB.

Step 5. Reconnect cable W134 to A4J1, then disconnect cable W135 at A4J2.

Step 6. Set up the 690XXA/691XXA to generate the CW frequencies listed in Table 5-12.

Table 5-12. *Coarse Loop Frequencies*

690XXA/691XXA CW Frequency	Measured Frequency at A4J3
2.010 GHz	205.0 MHz ±10 kHz
4.335 GHz	437.5 MHz ±10 kHz
8.780 GHz	980.0 MHz ±10 kHz

Step 7. Using a spectrum analyzer, measure the frequency and amplitude of the signal at A4J2 for each of the CW frequencies generated. In each case, the signal amplitude should be 0 dBm ±6 dB with sidebands at <–65 dBc.

- ❑ If the signals are correct in both frequency and amplitude, go to step 8.
- ❑ If the signals are incorrect, replace the A4 PCB.

Step 8. Reconnect cable W135 to A4J2 and run self-test again.

- ❑ If error 112 is not displayed, the problem is cleared.
- ❑ If error 112 is still displayed, contact your local ANRITSU service center for assistance.

Table 5-13. *Error Messages 113 and 115 (1 of 2)*

A7 YIG Loop

Error 113 YIG Loop Osc Failed
Error 115 Not Locked Indicator Failed

Description: Error 113 indicates that the YIG loop is not phase-locked. Error 115 indicates a failure of the not phased-lock indicator circuit.

Step 1. Verify the signal output from the A4 Coarse Loop PCB by performing steps 5 thru 7 in Table 5-11.

- ❑ If the coarse loop signals are correct in both frequency and amplitude, go to step 2.
- ❑ If the coarse loop signals are incorrect, replace the A4 PCB.

Step 2. Verify the signal output from the A5 Fine Loop PCB by performing the steps 5 thru 7 in Table 5-9.

- ❑ If the fine loop signals are correct in both frequency and amplitude, go to step 3.
- ❑ If the fine loop signals are incorrect, replace the A5 PCB.

Step 3. Disconnect the semi-rigid cable, W31, at output port J5 of the switched filter assembly.

Step 4. Set up the 690XXA/691XXA to generate a CW frequency of 2.000 GHz.

Step 5. Using a spectrum analyzer, measure the frequency and amplitude of the signal at J5 of the switched filter assembly. The frequency should be 2.000 GHz ±25 MHz and the amplitude should be from –20 to –27 dBm.

- ❑ If the signal is correct in both frequency and amplitude, go to step 6.
- ❑ If the signals are incorrect, replace the switched filter assembly.

Step 6. Repeat steps 4 and 5, incrementing the CW frequency in 1 GHz steps up to 20.000 GHz.

Step 7. If the signals from the coarse loop, fine loop, and switched filter assembly are all correct, replace the A7 YIG Loop PCB.

Table 5-13. *Error Messages 113 and 115 (2 of 2)*

Step 8. Run self-test.

- ❑ If error 113 or 115 are not displayed, the problem is cleared.
- ❑ If either error 113 or 115 are displayed, contact your local ANRITSU service center for assistance.

Table 5-14. *Error Message 114*

Down Converter

Error 114 Down Converter LO not Locked

Description: The local oscillator in the down converter assembly is not phase-locked.

Step 1. Disconnect cable W115 at A3J2.

Step 2. Using a spectrum analyzer, verify the presence of a +5 dBm ±6 dB, 500 MHz signal at A3J2.

- ❑ If present, go to step 3.
- ❑ If not present, replace the A3 PCB.

Step 3. Reconnect cable W115 to A3J1, then disconnect cable W115 at J2 of the down converter assembly.

Step 4. Using a spectrum analyzer, verify the presence of a +5 dBm ±6 dB, 500 MHz signal at the end of cable W115.

- ❑ If present, replace the down converter assembly.
- ❑ If not present, replace cable W115.

Table 5-15. *Error Message 116*

A11 FM PCB

Error 116 FM Loop Gain Check Failed

Description: The FM loop has failed or the loop gain is out of tolerance.

Step 1. Perform a preliminary calibration. (Refer to chapter 4 for the calibration procedure.)

Step 2. Run self-test.

- If error 116 is not displayed, the problem is cleared.
- If error 116 is still displayed, go to step 3.

Step 3. Replace the A11 PCB and run self-test again.

- If error 116 is not displayed, the problem is cleared.
- If error 116 is displayed, contact your local ANRITSU service center.

Table 5-16. *Error Messages 107, 117, 118, 119, and 120*

A12 Analog Instruction

Error 107 Sweep Time Check Failed
Error 117 Linearizer Check Failed
Error 118 Switchpoint DAC Failed
Error 119 Center Frequency Circuits Failed
Error 120 Delta-F Circuits Failed

Description: Each of these error messages indicates a problem in the circuitry on the A12 Analog Instruction PCB that provides frequency tuning voltages for the YIG-tuned oscillator.

Step 1. Perform a preliminary calibration. (Refer to chapter 4 for the calibration procedure.)

Step 2. Run self-test.

- If no error message is displayed, the problem is cleared.
- If any of the error messages, listed above, is displayed, go to step 3.

Step 3. Replace the A12 PCB and run self-test again.

- If no error message is displayed, the problem is cleared.
- If any of the error messages, listed above, is displayed, contact your local ANRITSU service center for assistance.

Table 5-17. *Error Messages 121, 122, 123, 127, 142, and 143 (1 of 2)*

A10 ALC

Error 121 Unleveled Indicator Failed
Error 122 Level Reference Failed
Error 123 Detector Log Amp Failed
Error 127 Detector Input Circuit Failed

Description: Error 121 indicates a failure of the circuit that alerts the CPU whenever the RF output power becomes unleveled. Each of the other error messages indicates a problem in the circuitry on the A10 ALC PCB that provides control of the RF output power level.

Step 1. Replace the A10 PCB, and run self-test.

- ❑ If no error message is displayed, the problem is cleared.
- ❑ If any of the error messages, listed above, is displayed, contact your local ANRITSU service center for assistance.

Error 142 Sample and Hold Circuit Failed

Description: Error 142 indicates a failure of the sample and hold circuitry on the A10 PCB. (This error occurs in 691XXA models only.)

Step 1. Set up the 691XXA as follows:

a. Modulation: Square Wave On
Source: Internal
Frequency: 400 Hz
Polarity: High RF On

Step 2. Using an oscilloscope, check for a 400 Hz square wave signal at A9TP13.

- ❑ If the signal is present, replace the A10 PCB.
- ❑ If the signal is not present, go to step 3.

Step 3. Using the oscilloscope, check for a 400 Hz square wave signal at A6TP3.

- ❑ If the signal is present, replace the A9 PCB.
- ❑ If the signal is not present, replace the A6 PCB.

Table 5-17. *Error Messages 121, 122, 123, 127, 142, and 143 (2 of 2)*

Error 143 Slope DAC Failed

Description: Error 143 indicates a problem with the level slope DAC circuitry on the A10 PCB.

NOTE

When troubleshooting this error in a 690XXA model, begin at step 3 of the procedure.

Step 1. Recalibrate the ALC slope. (Refer to chapter 4 for the calibration procedure.)

Step 2. Run self-test.

- ❑ If error 143 is not displayed, the problem is cleared.
- ❑ If error 143 is still displayed, go to step 3.

Step 3. Replace the A10 PCB and run self-test again.

- ❑ If error 143 is not displayed, the problem is cleared.
- ❑ If error 143 is still displayed, go to step 4.

Step 4. Replace the A12 PCB and run self-test again.

- ❑ If error 143 is not displayed, the problem is cleared.
- ❑ If error 143 is still displayed, contact your local ANRITSU service center for assistance.

Table 5-18. *Error Messages 124, 125, and 126 (1 of 2)*

YIG-tuned Oscillator

Error 124 Full Band Unlocked and Unleveled
Error 125 8.4-20 GHz Unlocked and Unleveled
Error 126 2-8.4 GHz Unlocked and Unleveled

Description: These error messages indicate either a failure of one or both of the oscillators in the 2-20 GHz YIG-tuned oscillator assembly.

Step 1. Connect a 562 Scalar Network Analyzer to the 690XXA/691XXA as follows:

- **a.** Connect the 690XXA/691XXA AUX I/O to the 562 AUX I/O.
- **b.** Connect the 562 DEDICATED GPIB to the 690XXA/691XXA IEEE-488 GPIB.
- **c.** Connect the RF Detector to the 562 Channel A Input.

Step 2. Set up the 690XXA/691XXA as follows:

- **a.** **690XXA Setup:**
  CW/SWEEP SELECT: Step
  F1: 2.000 GHz
  F2: 20.000 GHz
  Number of Steps: 400

  691XXA Setup:
  CW/SWEEP SELECT: Analog
  F1: 2.000 GHz
  F2: 20.000 GHz
  Sweep Time: 0.100 Sec

Step 3. Set up the 562 Scalar Network Analyzer as follows:

- **a.** Press SYSTEM MENU key.
- **b.** From System Menu display, select RESET.
- **c.** Press CHANNEL 2 DISPLAY: OFF
- **d.** Press CHANNEL 1 DISPLAY: ON
- **e.** Press CHANNEL 1 MENU key.
- **f.** From the Channel 1 Menu display, select POWER.

Step 4. Using the scalar network analyzer, measure the RF output directly at the YIG-tuned oscillator's output connector. The amplitude of the RF signal should be >+4 dBm throughout the full sweep.

Table 5-18. *Error Messages 124, 125, and 126 (2 of 2)*

- ❑ If the RF signal is correct in both frequency and amplitude throughout the full sweep, go to step 8.
- ❑ If there is no RF signal for all or part of the sweep or if the amplitude of the RF signal is low, go to step 5.

Step 5. Connect the X input of an oscilloscope to the 690XXA/691XXA rear panel HORIZ OUT connector.

Step 6. Using the oscilloscope, check for a –0.2 to –3.5 volt YIG tuning ramp at A13TP10.

- ❑ If the ramp signal is correct, go to step 7.
- ❑ If the ramp signal is incorrect or not present, replace the A13 PCB.

Step 7. Using the oscilloscope, check for the YIG bias voltages at the test points shown in Table 5-19.

- ❑ If the YIG bias voltages are correct, replace the YIG-tuned oscillator assembly.
- ❑ If the YIG bias voltages are incorrect, replace the A13 PCB.

Step 8. Run self-test again.

- ❑ If no error message is displayed, the problem is cleared.
- ❑ If any of the error messages, listed above, are displayed, contact your local ANRITSU service center for assistance.

Table 5-19. *YIG-tuned Oscillator Bias Voltages*

Test Point	YIG-tuned Oscillator Bias Voltages	
	2 to 8.4 GHz	8.4 to 20 GHz
A13TP3	+6V	+6V
A13TP5	0V	+8V
A13TP6	–5V	–5V
A13TP7	+8V	0V

Output Power Level Related Problems (0.01 to 20 GHz)

Error 128 .01-2 GHz Unleveled

Description: Error 128 indicates a failure of of the down converter leveling circuitry. The 690XXA/691XXA may or may not produce an RF output in the 0.01 to 2 GHz frequency range. Thus, there are two troubleshooting paths for this problem—unleveled with output power and unleveled with no/low output power.

Unleveled with output power (The warning message **UNLEVELED** appears on the front panel display):

Step 1. Set up the 690XXA/691XXA as follows:

a. 690XXA Setup:
CW/SWEEP SELECT: Step
F1: 0.010 GHz
F2: 2.000 GHz
Number of Steps: 400
L1: +1.00 dBm

691XXA Setup:
CW/SWEEP SELECT: Analog
F1: 0.010 GHz
F2: 2.000 GHz
Sweep Time: 0.100 Sec
L1: +1.00 dBm

b. LEVEL/ALC SELECT: ALC Mode
ALC Mode: Ext ALC Front
Leveling Menu: External Detector

Step 2. Connect a detector to the 690XXA/691XXA RF OUTPUT connector and connect the detected DC output of the detector to the front panel EXTERNAL ALC IN connector.

- If the warning message **UNLEVELED** no longer appears on the front panel display, replace the down converter.
- If the warning message **UNLEVELED** is still displayed, replace the A10 PCB.

Unleveled with no/low output power:

Step 1. Set up the 690XXA/691XXA as follows:

a. 690XXA Setup:
CW/SWEEP SELECT: Step
F1: 0.010 GHz
F2: 2.000 GHz
Number of Steps: 400
L1: +1.00 dBm

691XXA Setup:
CW/SWEEP SELECT: Analog
F1: 0.010 GHz
F2: 2.000 GHz
Sweep Time: 0.100 Sec
L1: +1.00 dBm

b. LEVEL/ALC SELECT: ALC Mode
Leveling Menu: Internal

Step 2. Connect the X input of an oscilloscope to the 690XXA/691XXA rear panel HORIZ OUT connector.

Step 3. Using the oscilloscope, check at the end of the cable that is connected to A10J3 for a >0.7 volt down converter detector output throughout the full sweep.

- ❑ If the detector voltage is correct, replace the A10 PCB.
- ❑ If the detector voltage is incorrect, go to step 4.

Step 4. Using the oscilloscope, check for a +15 volt down converter bias voltage at A13TP14.

- ❑ If the bias voltage is correct, go to step 5.
- ❑ If the bias voltage is not correct, replace the A13 PCB.

Step 5. Using the oscilloscope, check for a –2 volt PIN switch drive voltage at A9TP19 and A9TP22. If the 690XXA/691XXA has a SDM installed, also check for a +20 volt PIN switch drive voltage at A9TP9.

- ❑ If the PIN switch drive voltage(s) is correct, go to step 6.
- ❑ If the PIN switch drive voltage(s) is not correct, replace the A9 PCB.

Table 5-20. *Error Messages 128, 129, 130, 131, 132, 133, 134, and 135 (3 of 8)*

Step 6. Connect a 562 Scalar Network Analyzer to the 690XXA/691XXA as follows:

a. Connect the 690XXA/691XXA AUX I/O to the 562 AUX I/O.

b. Connect the 562 DEDICATED GPIB to the 690XXA/691XXA IEEE-488 GPIB.

c. Connect the RF Detector to the 562 Channel A Input.

Step 7. Set up the 562 Scalar Network Analyzer as follows:

a. Press SYSTEM MENU key.

b. From System Menu display, select RESET.

c. Press CHANNEL 2 DISPLAY: OFF

d. Press CHANNEL 1 DISPLAY: ON

e. Press CHANNEL 1 MENU key.

f. From the Channel 1 Menu display, select POWER.

Step 8. Using the scalar network analyzer, measure the RF output at J3 of the switched filter assembly. The amplitude of the RF signal should be >+17 dBm throughout the full sweep.

- If the amplitude of the RF signal is correct, replace the down converter assembly.
- If there is no RF signal or if the amplitude of the RF signal is low, replace the switched filter assembly.

Table 5-20. *Error Messages 128, 129, 130, 131, 132, 133, 134, and 135 (4 of 8)*

Error 129 Switched Filter or Level Detector Failed

Description: Error 129 indicates a failure of either the switched filter or level detector circuitry. The 690XXA/691XXA may or may not produce an RF output in the 2 to 20 GHz frequency range. Thus, there are two troubleshooting paths for this problem—unleveled with output power and unleveled with no/low output power.

Unleveled with output power (The warning message **UNLEVELED** appears on the front panel display):

Step 1. Set up the 690XXA/691XXA as follows:

a. 690XXA Setup:
CW/SWEEP SELECT: Step
F1: 0.010 GHz
F2: 20.000 GHz
Number of Steps: 400
L1: +1.00 dBm

691XXA Setup:
CW/SWEEP SELECT: Analog
F1: 0.010 GHz
F2: 20.000 GHz
Sweep Time: 0.100 Sec
L1: +1.00 dBm

b. LEVEL/ALC SELECT: ALC Mode
ALC Mode: Ext ALC Front
Leveling Menu: External Detector

Step 2. Connect a detector to the 690XXA/691XXA RF OUTPUT connector and connect the detected DC output of the detector to the front panel EXTERNAL ALC IN connector.

- If the warning message **UNLEVELED** no longer appears on the front panel display, replace the directional coupler.
- If the warning message **UNLEVELED** is still displayed, replace the A10 PCB.

Table 5-20. *Error Messages 128, 129, 130, 131, 132, 133, 134, and 135 (5 of 8)*

Unleveled with no/low output power:

Step 1. Set up the 690XXA/691XXA as follows:

a. 690XXA Setup:
CW/SWEEP SELECT: Step
F1: 0.010 GHz
F2: 20.000 GHz
Number of Steps: 400
L1: +1.00 dBm

691XXA Setup:
CW/SWEEP SELECT: Analog
F1: 0.010 GHz
F2: 20.000 GHz
Sweep Time: 0.100 Sec
L1: +1.00 dBm

b. LEVEL/ALC SELECT: ALC Mode
Leveling Menu: Internal

Step 2. Connect the X input of an oscilloscope to the 690XXA/691XXA rear panel HORIZ OUT connector.

Step 3. Using the oscilloscope, check the switched filter bias voltages at A13TP4 and A13TP9. The bias voltage at A13TP4 should be +6 volts; the bias voltage at A13TP9 should be +8 volts. If the 690XXA/691XXA has a SDM installed, also check for a +20 volt PIN switch drive voltage at A9TP9.

- ❑ If the bias and the PIN switch drive voltages are correct, go to step 4.
- ❑ If the bias voltages are not correct, replace the A13 PCB.
- ❑ If the PIN switch drive voltage is not correct, replace the A9 PCB.

Step 4. Connect a 562 Scalar Network Analyzer to the 690XXA/691XXA as follows:

a. Connect the 690XXA/691XXA AUX I/O to the 562 AUX I/O.

b. Connect the 562 DEDICATED GPIB to the 690XXA/691XXA IEEE-488 GPIB.

c. Connect the RF Detector to the 562 Channel A Input.

Table 5-20. *Error Messages 128, 129, 130, 131, 132, 133, 134, and 135 (6 of 8)*

Step 5. Set up the 562 Scalar Network Analyzer as follows:

a. Press SYSTEM MENU key.

b. From System Menu display, select RESET.

c. Press CHANNEL 2 DISPLAY: OFF

d. Press CHANNEL 1 DISPLAY: ON

e. Press CHANNEL 1 MENU key.

f. From the Channel 1 Menu display, select POWER.

Step 6. Using the scalar network analyzer, measure the RF output at J2 of the switched filter assembly. The amplitude of the RF signal should be >+15 dbm (>+20 dBm with Option 15A) throughout the full sweep.

- ❑ If the amplitude of the RF signal is correct, check for bad cables.
- ❑ If there is no RF signal or if the amplitude of the RF signal is low, replace the switched filter assembly.

Table 5-20. *Error Messages 128, 129, 130, 131, 132, 133, 134, and 135 (7 of 8)*

Error 130 2-3.3 GH Switched Filter
Error 131 3.3-5.5 GH Switched Filter
Error 132 5.5-8.4 GH Switched Filter
Error 133 8.4-13.25 GH Switched Filter
Error 134 13.25-20 GH Switched Filter

Description: Each of these error messages indicates a failure in a switched filter path within the switched filter assembly. The 690XXA/691XXA may or may not produce an RF output in the frequency range of the failed switched filter path.

Step 1. Set up the 690XXA/691XXA as follows:

a. 690XXA Setup:
CW/SWEEP SELECT: Step
F1: 2.000 GHz
F2: 20.000 GHz
Number of Steps: 400

691XXA Setup:
CW/SWEEP SELECT: Analog
F1: 2.000 GHz
F2: 20.000 GHz
Sweep Time: 0.100 Sec

Step 2. Connect the X input of an oscilloscope to the 690XXA/691XXA rear panel HORIZ OUT connector.

Step 3. Using the oscilloscope, check for the switched filter PIN switch drive voltages at the test points shown in Table 5-21.

- If the PIN switch drive voltages are correct, replace the switched filter assembly.
- If the PIN switch drive voltages are incorrect, replace the A9 PCB.

Table 5-21. *Switched Filter PIN Switch Drive Voltages*

Test Point	Active Frequency Range	Active Voltage	Inactive Voltage
A9TP18	2 to 3.3 GHz	–2V	+1V
A9TP10	3.3 to 5.5 GHz	–2V	+1V
A9TP12	5.5 to 8.4 GHz	–2V	+1V
A9TP16	8.4 to 13.25 GHz	–2V	+1V
A9TP21	13.25 to 20 GHz	–2V	+1V
A9TP17	2 to 8.4 GHz	–2V	+2V

Table 5-20. *Error Messages 128, 129, 130, 131, 132, 133, 134, and 135 (8 of 8)*

Error 135 Modulator or Driver Failed

Description: Error 135 indicates a failure of the modulator in the switched filter assembly or the modulator driver circuitry on the A9 PIN Control PCB.

Step 1. Replace the A9 PCB and run self-test.

- If error 135 is not displayed, the problem is cleared.
- If error 135 is still displayed, go to step 2.

Step 2. Replace the switched filter assembly and run self-test again.

- If error 135 is not displayed, the problem is cleared.
- If error 135 is still displayed, contact your local ANRITSU service center for assistance.

Table 5-22. *Error Messages 138, 139, 140, and 141 (1 of 2)*

Output Power Level Related Problems (20 to 40 GHz) 690XXA/691XXA Models with SDM

Error 138 SDM Unit or Driver Failed

Description: Error 138 indicates a failure of the SDM, a failure of the SDM bias regulator circuitry on the A14 SDM, SQM Driver PCB, or a failure of the frequency band selection circuitry on the A12 Analog Instruction PCB. The 690XXA/691XXA will not produce an RF output in the 20 to 40 GHz frequency range.

Step 1. Set up the 690XXA/691XXA as follows:

a. 690XXA Setup:
CW/SWEEP SELECT: Step
F1: 20.000 GHz
F2: 40.000 GHz
Number of Steps: 400
L1: +1.00 dBm

691XXA Setup:
CW/SWEEP SELECT: Analog
F1: 20.000 GHz
F2: 40.000 GHz
Sweep Time: 0.100 Sec
L1: +1.00 dBm

Step 2. Connect the X input of an oscilloscope to the 690XXA/691XXA rear panel HORIZ OUT connector.

Step 3. Using the oscilloscope, check for a +8 volts SDM bias voltage at A14TP2 throughout the full sweep.

- ❑ If the SDM bias voltage is correct, replace the SDM.
- ❑ If the SDM bias voltage is not correct, go to step 4.

Step 4. Replace the A14 PCB and run self-test again.

- ❑ If error 138 is not displayed, the problem is cleared.
- ❑ If error 138 is still displayed, go to step 5.

Step 5. Replace the A12 PCB and run self-test again.

- ❑ If error 138 is not displayed, the problem is cleared.
- ❑ If error 138 is still displayed, contact your local ANRITSU service center for assistance.

Table 5-22. *Error Messages 138, 139, 140, and 141 (2 of 2)*

Error 139 32-40 GHz SDM Section Failed
Error 140 25-32 GHz SDM Section Failed
Error 141 20-25 GHz SDM Section Failed

Description: Each of these error messages indicates a failure in a switched doubler filter path within the SDM. The 690XXA/691XXA will not produce an RF output in the frequency range of the failed switched doubler filter path.

Step 1. Set up the 690XXA/691XXA as follows:

a. 690XXA Setup:
CW/SWEEP SELECT: Step
F1: 2.000 GHz
F2: 40.000 GHz
Number of Steps: 400
L1: +1.00 dBm

691XXA Setup:
CW/SWEEP SELECT: Analog
F1: 2.000 GHz
F2: 40.000 GHz
Sweep Time: 0.100 Sec
L1: +1.00 dBm

Step 2. Connect the X input of an oscilloscope to the 690XXA/691XXA rear panel HORIZ OUT connector.

Step 3. Using the oscilloscope, check the PIN switch drive voltages at A9TP11, A9TP15, and A9TP24 (shown in Table 5-23).

- ❑ If the PIN switch drive voltages are correct, replace the SDM.
- ❑ If the PIN switch drive voltages are not correct, replace the A9 PCB.

Table 5-23. *SDM PIN Switch Drive Voltages*

Test Point	Active Frequency Range	Active Voltage	Inactive Voltage
A9TP9	0.01 to 20 GHz	+20V	–15V
A9TP11	20 to 25 GHz	+20V	–15V
A9TP15	25 to 32 GHz	+20V	–15V
A9TP24	32 to 40 GHz	+20V	–15V

Table 5-24. *Error Message 144*

Error 144 RF was Off when Selftest started. Some tests where not performed

Description: Indicates that some self-tests were not performed because the RF Output was selected OFF on the front panel.

Step 1. Press the OUTPUT key on the front panel to turn the RF Output ON.

Step 2. Run self-test again.

Chapter 6
Removal and Replacement Procedures

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Table of Contents (Continued)

Chapter 6
Removal and Replacement Procedures

6-1 INTRODUCTION

This chapter provides procedures for gaining access to the major 690XXA/691XXA assemblies, subassemblies, and components for troubleshooting or replacement.

WARNING

Hazardous voltages are present inside the 690XXA/691XXA whenever ac line power is connected. Turn off the unit and remove the line cord before removing any covers or panels. Troubleshooting and repair procedures should only be performed by service personnel who are fully aware of the potential hazards.

CAUTION

Many subassemblies in the instrument contain static-sensitive components. Improper handling of these subassemblies may result in damage to the components. ***Always*** observe the static-sensitive component handling procedures described in Chapter 1, Figure 1-4.

6-2 REMOVING AND REPLACING THE CHASSIS COVERS

Troubleshooting procedures require removal of the top cover. Replacement of some 690XXA/691XXA assemblies and parts require removal of all covers. The following procedure describes this process.

Preliminary Disconnect the power cord from the unit.

Procedure Remove and replace the chassis covers as follows:

Step 1 Using a Phillips screwdriver, remove the screws and the two feet from the top corners at the rear of the instrument (Figure 6-1).

Step 2 Remove the screw that fastens the top cover to the chassis. (The screw is located at the rear of the instrument.)

Step 3 Slide the top cover out along the grooves in the chassis and set it aside.

Step 4 Turn the instrument over so that the bottom cover is on top.

Step 5 Remove the screws and the two feet from the bottom corners at the rear of the instrument.

Step 6 Remove the screw that fastens the bottom cover to the chassis. (The screw is located at the rear of the instrument.)

Step 7 Slide the bottom cover out along the grooves in the chassis and set it aside.

Step 8 Turn the instrument over to return it to the upright position.

Step 9 Remove the screws and the carrying handle from the side handle cover. (The two screws fastening the carrying handle through the side handle cover to the chassis are accessable by lifting up the rubber covering at the each end of the handle.)

Step 10 Remove the screw that fastens the side handle cover to the chassis. (The screw is located at the rear of the instrument.)

Step 11 Remove the side handle cover and set it aside.

NOTE

The screws with green heads have metric threads. When it becomes necessary to replace any of these screws, *always* use the exact replacement green-headed screws (ANRITSU P/N 2000-560) to avoid damage to the instrument.

Step 12 Remove the screw that fastens the other side cover to the chassis. (The screw is located at the rear of the instrument.)

Step 13 Remove the side cover and set it aside.

Step 14 To replace the chassis covers, reverse the procedure used to remove them.

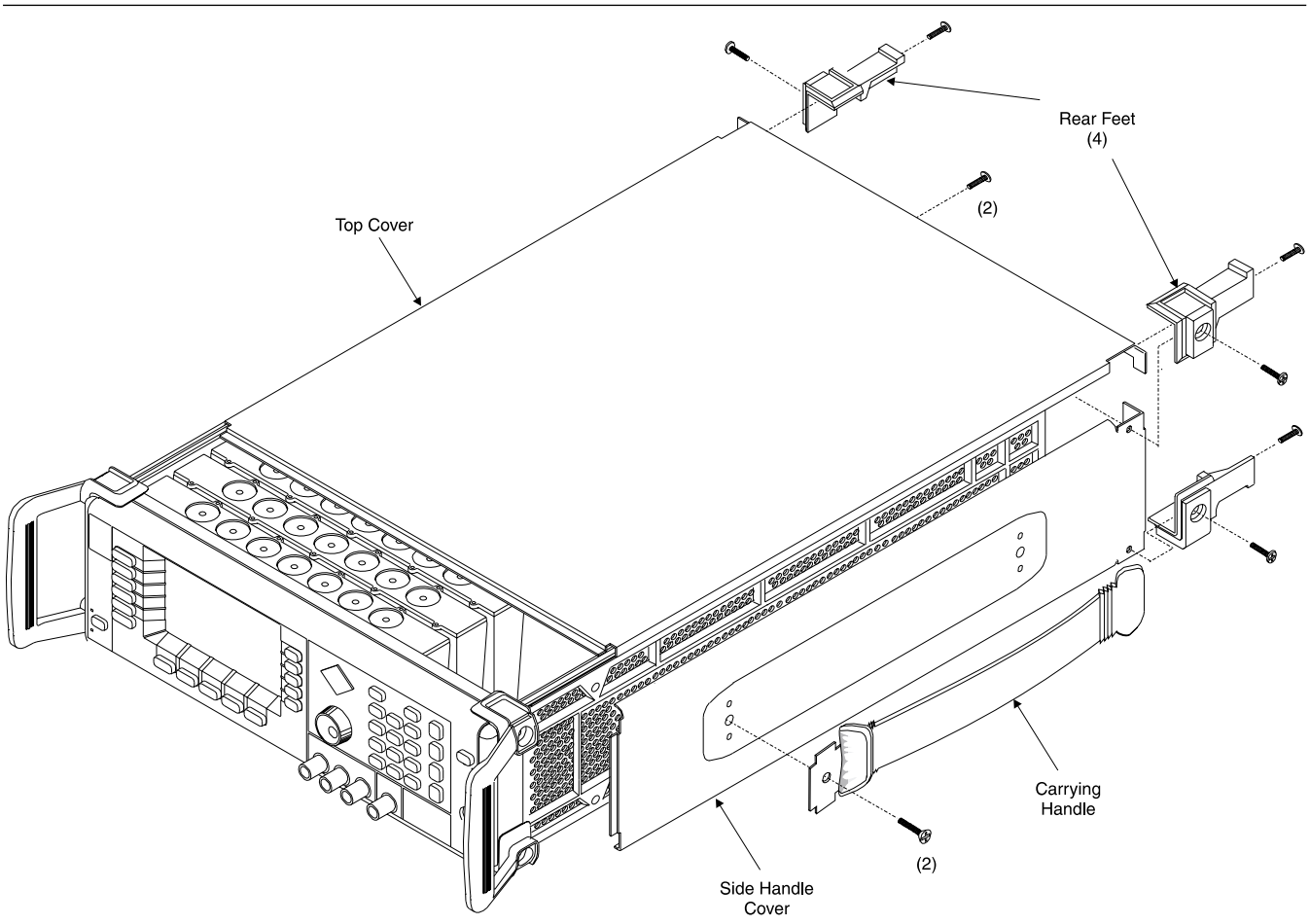

Figure 6-1. *Chassis Covers Removal*

6-3 REMOVING AND REPLACING THE FRONT PANEL ASSEMBLY

This paragraph provides instructions for removing and replacing the front panel assembly of the 690XXA/691XXA. The front panel assembly contains the A1 and A2 Front Panel PCBs. Refer to Figure 6-2 during this procedure.

Preliminary Disconnect the power cord from the unit and remove the chassis covers as described in paragraph 6-2.

Procedure Remove and replace the front panel assembly as follows:

> **NOTE**
> The screws with green heads have metric threads. When it becomes necessary to replace any of these screws, *always* use the exact replacement green-headed screws (ANRITSU P/N 2000-560) to avoid damage to the instrument.

Step 1 Using a Phillips screwdriver, remove the screws and the front handle assemblies from the instrument. (For instruments not having front handles, remove the screws and the front top and bottom feet from the instrument.)

Step 2 Remove the rotary knob from the front panel by pulling straight out on it.

Step 3 Carefully pull the front panel away from the chassis until the screws attaching the front panel assembly to the chassis are accessable.

Step 4 Remove the screws attaching the front panel assembly to the chassis sides.

Step 5 Disconnect the front panel ribbon cables from connectors J1 and J22 of the Motherboard.

Step 6 Turn the instrument upside down.

Step 7 Remove the screw attaching the front panel assembly to the chassis pan.

Step 8 Carefully pull the front panel assembly forward until it is clear of the RF OUTPUT connector.

Step 9 If installed, disconnect the coaxial cable from the front panel assembly connector A2J13 (FM input) by pulling straight out on the cable connector.

Step 10 To replace the front panel assembly, reverse the removal process.

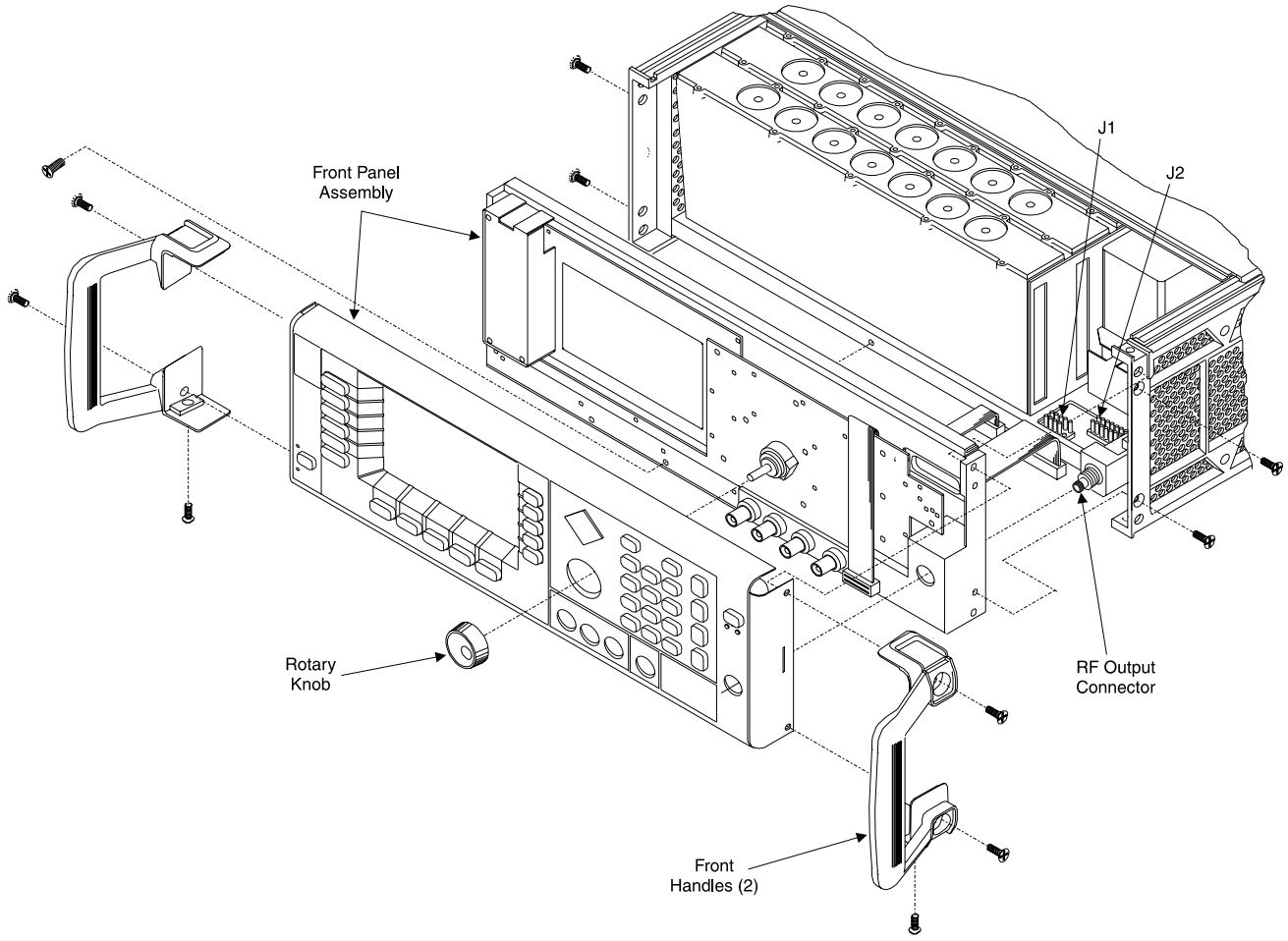

Figure 6-2. *Front Panel Assembly Removal*

6-4 REMOVING AND REPLACING THE A3, A5, OR A6 PCB

This paragraph provides instructions for removing and replacing the A3 Reference Loop PCB, the A5 Fine Loop PCB, or the A6 Square Wave Generator PCB, all of which are located in the RF housing (see Figure 6-3).

Preliminary Disconnect the power cord from the unit and remove the top cover as described in paragraph 6-2.

Procedure Remove and replace the A3, A5, or A6 PCB as follows:

Step 1 Disconnect the coaxial cables from the PCB to be removed by lifting up on the cable connectors.

Step 2 Using a Phillips screwdriver, remove the nine screws that retain the RF housing cover and set aside.

Step 3 Remove the RF housing cover and set aside.

Step 4 Lift up on the edge tabs of the PCB and lift it out of the RF housing.

Step 5 Remove the “O” rings installed on each MCX connector and retain them for use on the replacement PCB.

Step 6 To replace the PCB, reverse the removal process.

6-5 REMOVING AND REPLACING THE A4 PCB

This paragraph provides instructions for removing and replacing the A4 Coarse Loop PCB, which is located in the RF housing (Figure 6-3).

Preliminary Disconnect the power cord from the unit and remove the top and bottom covers as described in paragraph 6-2.

Procedure Remove and replace the A4 PCB as follows:

Step 1 Disconnect the coaxial cables for the PCB by lifting up on the cable connectors.

Step 2 Turn the instrument over so that the bottom is on top.

Step 3 Using a Phillips screwdriver, remove the four screws that fasten the PCB to the chassis pan.

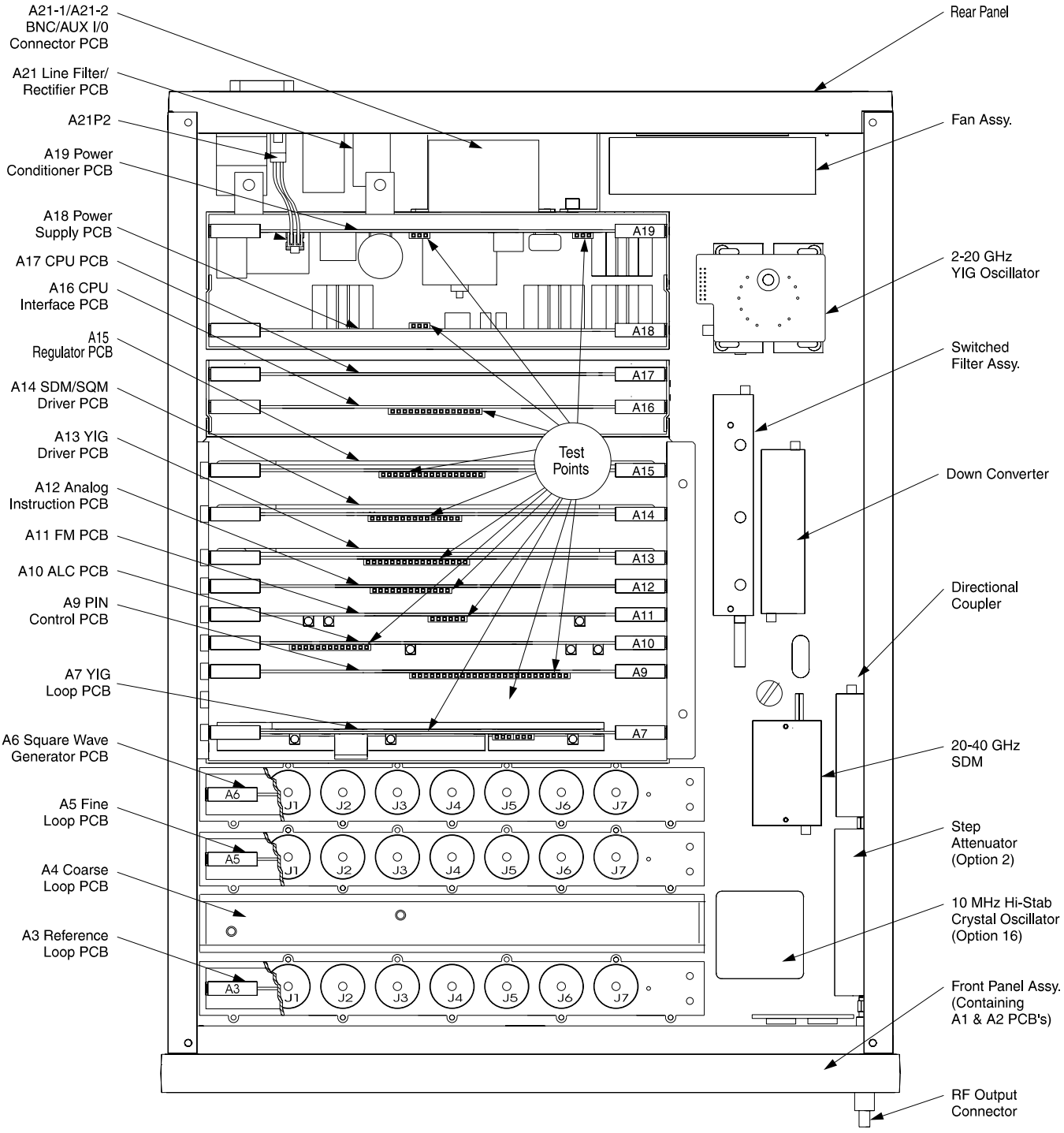

Figure 6-3. *Assembly and Component Locator Diagram*

Step 4 Turn the instrument over to return it to the upright position.

Step 5 Lift the A4 PCB out of the RF housing.

Step 6 To replace the PCB, reverse the removal process.

6-6 REMOVING AND REPLACING THE A7 PCB

This paragraph provides instructions for removing and replacing the A7 YIG Loop PCB, which is located in the main card cage (see Figure 6-3).

Preliminary Disconnect the power cord from the unit and remove the top cover as described in paragraph 6-2.

Procedure Remove and replace the A7 PCB as follows:

Step 1 Remove the main card cage cover and set aside.

Step 2 Using a $\frac{5}{16}$-inch wrench, disconnect coaxial cable W31 from the Sampler/SRD module on the PCB.

Step 3 Disconnect the coaxial cables at A7J1 and A7J5 by lifting up on the cable connectors.

Step 4 Lift up on the edge tabs of the PCB and lift it out of the card cage.

Step 5 To replace the A7 PCB, reverse the removal process.

6-7 REMOVING AND REPLACING THE A9, A10, A11, OR A12 PCB

This paragraph provides instructions for removing and replacing the A9 PIN Control PCB, the A10 ALC PCB, the A11 FM PCB, or the A12 Analog Instruction PCB, all of which are located in the main card cage (see Figure 6-3).

Preliminary Disconnect the power cord from the unit and remove the top cover as described in paragraph 6-2.

Procedure Remove and replace the A9, A10, A11, or A12 PCB as follows:

Step 1 Remove the main card cage cover and set aside.

Step 2 Disconnect any coaxial cables from the PCB by lifting up on the cable connectors.

Step 3 Lift up on the edge tabs of the PCB and lift it out of the card cage.

Step 4 To replace the PCB, reverse the removal process.

6-8 REMOVING AND REPLACING THE A13, A14, OR A15 PCB

This paragraph provides instructions for removing and replacing the A13 YIG Driver PCB, the A14 SDM, SQM Driver PCB, or the A15 Regulator PCB, all of which are located in the main card cage (see Figure 6-3). Each of these PCB assemblies consists of a PCB and a PCB Heat Sink subassembly.

Preliminary Disconnect the power cord from the unit and remove the top cover as described in paragraph 6-2.

Procedure Remove and replace the A13, A14, or A15 PCB as follows:

Step 1 Remove the main card cage cover and set aside.

Step 2 Lift up on the edge tabs of the PCB and lift it out of the card cage.

Step 3 Using a Phillips screwdriver, remove the two screws that fasten the PCB Heat Sink subassembly to the chassis pan.

Step 4 Lift the PCB Heat Sink subassembly out of the card cage.

Step 5 To replace the PCB, reverse the removal process.

6-9 REMOVING AND REPLACING THE A16 OR A17 PCB

This paragraph provides instructions for removing and replacing the A16 CPU Interface PCB or the A17 CPU PCB, both of which are located in the CPU housing assembly (see Figure 6-3).

Preliminary Disconnect the power cord from the unit and remove the top cover as described in paragraph 6-2.

Procedure Remove and replace the A16 or A17 PCB as follows:

Step 1 Remove the CPU cover and set aside.

Step 2 Lift up on the edge tabs of the PCB and lift it out of the CPU housing.

Step 3 To replace the PCB, reverse the removal process.

6-10 REMOVING AND REPLACING THE A18 OR A19 PCB

This paragraph provides instructions for removing and replacing the A18 Power Supply PCB or the A19 AC Line Conditioner PCB, both of which are located in the power supply housing assembly (see Figure 6-3).

Preliminary Disconnect the power cord from the unit and remove the top cover as described in paragraph 6-2.

WARNING

When power is removed from the instrument, ***always*** allow five minutes for the capacitors on the A21 Line Filter/Rectifier PCB to discharge before removing either the A18 or A19 PCB.

Procedure Remove and replace the A18 or A19 PCB as follows:

Step 1 Remove the power supply cover and set it aside.

Step 2 If the A19 PCB is being removed, (1) disconnect the cable assembly from the A21 Line Filter/Rectifier PCB at A19P2 and (2) remove the Nylatch fastener used to connect the PCB to the housing assembly.

Step 3 Lift up the edge tabs on the PCB and lift it out of the power supply housing.

Step 4 To replace the PCB, reverse the removal process.

6-11 REMOVING AND REPLACING THE REAR PANEL ASSEMBLY

This paragraph provides instructions for removing and replacing the rear panel assembly of the 690XXA/691XXA. The rear panel assembly contains the A21 Line Filter/Rectifier PCB, the A21-1/A21-2 BNC/AUX I/O Connector PCB, the line module assembly, and the fan assembly. Refer to Figure 6-4 during this procedure.

Preliminary Disconnect the power cord from the unit and remove the chassis covers as described in paragraph 6-2.

WARNING

When power is removed from the instrument, ***always*** allow five minutes for the capacitors on the A21 Line Filter/Rectifier PCB to discharge before removing the rear panel assembly.

Procedure Remove and replace the rear panel assembly as follows:

Step 1 Using a Phillips screwdriver, remove the screw on the top of the rear panel assembly that fastens the rear panel assembly to the bracket attached to the power supply housing.

Step 2 Turn the instrument upside down.

Step 3 Remove the three screws from the rear panel assembly. (One screw fastens the rear panel assembly to the bracket attached to the power supply housing; the other two screws attach the rear panel assembly to the Motherboard.)

Step 4 Return the instrument to the upright position.

Step 5 Remove the screws attaching the rear panel assembly to the chassis sides.

Step 6 Using a $\frac{7}{16}$-inch wrench, disconnect the coaxial cables going to the rear panel 10 MHz REF IN, 10 MHz REF OUT, and FM IN (if installed) BNC connectors.

Step 7 Remove the power supply cover and set it aside.

Step 8 Disconnect the cable assembly from the A21 Line Filter/Rectifier PCB at connector P2 on the A19 PCB.

Step 9 Carefully pull the rear panel assembly away from the 690XXA/691XXA chassis until the cable connections to the Motherboard are accessable.

Step 10 Disconnect the fan cable connector from J13 on the Motherboard.

Step 11 Disconnect the A21-1/A21-2 PCB ribbon cable connector from J14 on the Motherboard.

Step 12 Disconnect the GPIB cable connector from J16 on the Motherboard.

Step 13 Carefully pull the rear panel assembly completely free from the 690XXA/691XXA chassis.

Step 14 To replace the rear panel assembly, reverse the removal process.

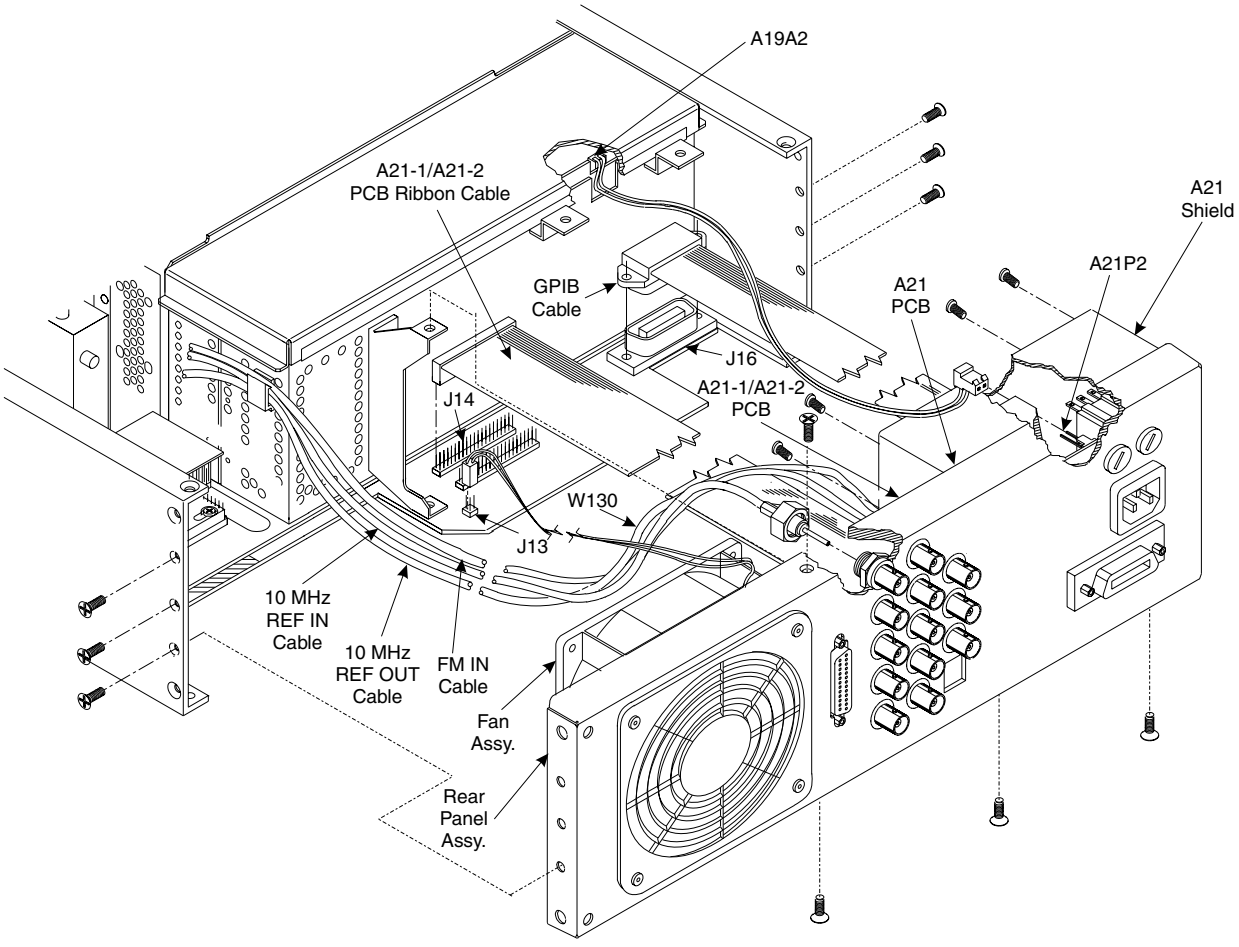

Figure 6-4. *Rear Panel Assembly Removal*

6-12 REMOVING AND REPLACING THE A21 PCB

This paragraph provides instructions for removing and replacing the A21 Line Filter/Rectifier PCB, which is located on the rear panel assembly (see Figure 6-4).

Preliminary Disconnect the power cord from the unit. Remove the chassis covers as described in paragraph 6-2. Remove the rear panel assembly as described in paragraph 6-10.

WARNING

When power is removed from the instrument, ***always*** allow five minutes for the capacitors on the A21 Line Filter/Rectifier PCB to discharge before removing the rear panel assembly.

Procedure Remove and replace the A21 PCB as follows:

Step 1 Using a Phillips screwdriver, remove the four screws that fasten the A21 shield to the A21 PCB.

Step 2 Remove the shield and set it aside.

Step 3 Disconnect the cables connected to P1, P2, and P6 on the PCB.

Step 4 Using a Phillips screwdriver, remove the four screws that fasten the PCB to the rear panel assembly and set aside.

Step 5 Remove the PCB from the rear panel assembly.

Step 6 To replace the PCB, reverse the removal process.

6-13 REMOVING AND REPLACING THE A21-1/A21-2 PCB

This paragraph provides instructions for removing and replacing the A21-1/A21-2 BNC/AUX I/O Connector PCB, which is located on the rear panel assembly (see Figures 6-4). The 691XXA has the A21-1 BNC/AUX I/O Connector PCB; the 690XXA has the A21-2 BNC/AUX I/O Connector PCB.

Preliminary Disconnect the power cord from the unit. Remove the chassis covers as described in paragraph 6-2. Remove the rear panel assembly as described in paragraph 6-10.

WARNING

When power is removed from the instrument, ***always*** allow five minutes for the capacitors on the A21 Line Filter/Rectifier PCB to discharge before removing the A21-1/A21-2 PCB.

Procedure Remove and replace the A21-1/A21-2 PCB as follows:

Step 1 Using a Phillips screwdriver, remove the four screws that fasten the A21 shield to the A21 PCB.

Step 2 Remove the shield and set it aside.

Step 3 Disconnect the ribbon cable connector from the A21-1/A21-2 PCB.

Step 4 Using a ANRITSU P/N T1451 tool, remove the dress nuts from the rear panel BNC connectors. (The A21-1 PCB has 11 BNC connectors; the A21-2 PCB has 5 BNC connectors.)

Step 5 Carefully remove the A21-1/A21-2 PCB from the rear panel assembly.

Step 6 To replace the PCB, reverse the removal process.

6-14 REMOVING AND REPLACING THE FAN ASSEMBLY

This paragraph provides instructions for removing and replacing the fan assembly, which is located on the rear panel assembly (see Figure 6-4).

Preliminary Disconnect the power cord from the unit. Remove the chassis covers as described in paragraph 6-2. Remove the rear panel assembly as described in paragraph 6-10.

WARNING

When power is removed from the instrument, ***always*** allow five minutes for the capacitors on the A21 Line Filter/Rectifier PCB to discharge before removing the rear panel assembly.

Procedure Remove and replace the fan assembly as follows:

Step 1 With the rear panel laying flat, use a Phillips screwdriver to remove the four screws and flat washers that fasten the fan mount to the rear panel.

Step 2 Lift the fan mount, containing the fan assembly, from the rear panel assembly.

Step 3 Remove the fan assembly from the fan mount.

Step 4 Clean the honeycomb fan filter as required before replacing the fan assembly.

Step 5 To replace the fan assembly, reverse the removal process.

NOTE

To ensure proper cooling of the unit, ***always*** mount the fan assembly with the airflow direction indicator arrow on the fan body pointing toward the interior of the instrument.

Appendix A
Test Records

A-1 INTRODUCTION

This appendix provides test records for recording the results of the Performance Verification tests (Chapter 3) and the Calibration procedures (Chapter 4). They jointly provide the means for maintaining an accurate and complete record of instrument performance. Test records are provided for all models of the Series 690XXA/691XXA Synthesized CW/Sweep Generators. Table A-1 provides the location of each test record in this appendix.

Each test record has been customized to cover a particular 690XXA/691XXA model. It contains specific references to frequency parameters and power levels that are applicable only to that instrument model and its available options.

We recommend that you make a copy of these pages each time the test procedures are performed. By dating each Test Record copy, a detailed history of instrument performance can be accumulated.

Table A-1. *Test Record Index*

Model Number	Performance Verification	Calibration
69037A/69137A	A-3 thru A-11	A-13 thru A-15
69045A/69145A	A-17 thru A-26	A-27 thru A-29
69047A/69147A	A-31 thru A-40	A-41 thru A-43
69053A/69153A	A-45 thru A-54	A-55 thru A-57
69055A/69155A	A-59 thru A-69	A-71 thru A-73
69059A/69159A	A-75 thru A-85	A-87 thru A-89
69063A/69163A	A-91 thru A-100	A-101 thru A-103
69065A/69165A	A-105 thru A-115	A-117 thru A-119
69069A/69169A	A-121 thru A-131	A-133 thru A-135
69075A/69175A	A-137 thru A-145	A-147 thru A-149
69077A/69177A	A-151 thru A-159	A-161 thru A-163
69085A/69185A	A-165 thru A-173	A-175 thru A-177
69087A/69187A	A-179 thru A-187	A-189 thru A-191
69095A/69195A	A-193 thru A-200	A-201 thru A-203
69097A/69197A	A-205 thru A-212	A-213 thru A-215

ANRITSU Model 69037A/69137A **Date:** _____

Serial Number _____ **Tested By:** _____

3-6 Internal Time Base Aging Rate Test

Test Procedure	Measured Value	Upper Limit
Record frequency error value	_____	
Record frequency error value (after 24 hours)	_____	
Record the computed aging rate	_____per day	$2x10^{-8}$ per day ($5x10^{-10}$ per day with Option 16)

3-7 Frequency Synthesis Tests

Coarse Loop/YIG Loop Test Procedure

Test Frequency (in GHz)	Measured Value *
2.000 000 000	_____
3.000 000 000	_____
4.000 000 000	_____
5.000 000 000	_____
6.000 000 000	_____
7.000 000 000	_____
8.000 000 000	_____
9.000 000 000	_____
10.000 000 000	_____
11.000 000 000	_____
12.000 000 000	_____
13.000 000 000	_____
14.000 000 000	_____
15.000 000 000	_____
16.000 000 000	_____
17.000 000 000	_____
18.000 000 000	_____
19.000 000 000	_____
20.000 000 000	_____

* Specification for all frequencies listed above is ±100 Hz

Fine Loop Test Procedure (Standard 69X37A)

Test Frequency (in GHz)	Measured Value **
2.000 001 000	_____
2.000 002 000	_____
2.000 003 000	_____
2.000 004 000	_____
2.000 005 000	_____
2.000 006 000	_____
2.000 007 000	_____
2.000 008 000	_____
2.000 009 000	_____
2.000 010 000	_____

** Specification for all frequencies listed above is ±100 Hz

Fine Loop Test Procedure (69X37A with Option 11)

Test Frequency (in GHz)	Measured Value ***
2.000 000 100	_____
2.000 000 200	_____
2.000 000 300	_____
2.000 000 400	_____
2.000 000 500	_____
2.000 000 600	_____
2.000 000 700	_____
2.000 000 800	_____
2.000 000 900	_____
2.000 001 000	_____

*** Specification for all frequencies listed above is ±10 Hz

3-8 Spurious Signals Test: RF Output Signals <2 GHz

This test is not applicable to the 69037A/69137A model.

3-9 Harmonic Test: RF Output Signals From 2 to 20 GHz

Test Procedure (2 to 10 GHz)	**Measured Value**	**Upper Limit**
Set F1 to 2.1 GHz Record the level of all harmonics of the 2.1 GHz carrier:		
4.2 GHz (2nd harmonic)	_____dBc	–60 dBc*
6.3 GHz (3rd harmonic)	_____dBc	–60 dBc*
8.4 GHz (4th harmonic)	_____dBc	–60 dBc*
10.5 GHz (5th harmonic)	_____dBc	–60 dBc*
12.6 GHz (6th harmonic)	_____dBc	–60 dBc*
14.7 GHz (7th harmonic)	_____dBc	–60 dBc*
16.8 GHz (8th harmonic)	_____dBc	–60 dBc*
18.9 GHz (9th harmonic)	_____dBc	–60 dBc*
Set F1 to 3.6 GHz Record the level of all harmonics of the 3.6 GHz carrier:		
7.2 GHz (2nd harmonic)	_____dBc	–60 dBc*
10.8 GHz (3rd harmonic)	_____dBc	–60 dBc*
14.4 GHz (4th harmonic)	_____dBc	–60 dBc*
18.0 Ghz (5th harmonic)	_____dBc	–60 dBc*
Set F1 to 7.0 GHz Record the level of all harmonics of the 7 GHz carrier:		
14.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 10.0 GHz Record the level of all harmonics of the 10 GHz carrier:		
20.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc if Option 15A (High Power) installed.

3-9 Harmonic Test: RF Output Signals From 2 to 20 GHz (Continued)

Test Procedure (11 to 20 GHz)	Measured Value	Upper Limit
Set F1 to 12.4 GHz Record the level of all harmonics of the 12.4 GHz carrier:		
24.8 GHz (2nd harmonic)	_____dBc	–60 dBc*
37.2 GHz (3rd harmonic)	_____dBc	–60 dBc*
Set F1 to 16.0 GHz Record the level of all harmonics of the 16.0 GHz carrier:		
32.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 20.0 GHz Record the level of all harmonics of the 20.0 GHz carrier:		
40.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc is Option 15A (High Power) installed.

3-10 Single Sideband Phase Noise Test

Test Procedure	Measured Value	Upper Limit
Set F1 to 2.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–77 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 6.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–75 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 10.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–71 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 20.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–63 dBc
1 kHz	_____dBc	–92 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc

3-11 Power Level Accuracy and Flatness Tests (Model 69037A/69137A without Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz

Set L1 to:	**Measured Power ***
+13 dBm	_____dBm
+12 dBm	_____dBm
+11 dBm	_____dBm
+10 dBm	_____dBm
+ 9 dBm	_____dBm
+ 8 dBm	_____dBm
+ 7 dBm	_____dBm
+ 6 dBm	_____dBm
+ 5 dBm	_____dBm
+ 4 dBm	_____dBm
+ 3 dBm	_____dBm
+ 2 dBm	_____dBm
+ 1 dBm	_____dBm

* Specification is ±1.0 dB.

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+13.0 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69137A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+13 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69037A/69137A with Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz

Set L1 to:	Measured Power *
+11 dBm	_____dBm
+10 dBm	_____dBm
+ 9 dBm	_____dBm
+ 8 dBm	_____dBm
+ 7 dBm	_____dBm
+ 6 dBm	_____dBm
+ 5 dBm	_____dBm
+ 4 dBm	_____dBm
+ 3 dBm	_____dBm
+ 2 dBm	_____dBm
+ 1 dBm	_____dBm
+ 0 dBm	_____dBm
– 1 dBm	_____dBm

* Specification is ±1.0 dB.

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+11 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69137A only)

Set L1 to:	Max Power	Min Power	Variation ***
+11 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 6.0 dB (typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69037A/69137A with Option 15A High Power & without Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz

Set L1 to:	**Measured Power ***
+17 dBm	_____dBm
+16 dBm	_____dBm
+15 dBm	_____dBm
+14 dBm	_____dBm
+13 dBm	_____dBm
+12 dBm	_____dBm
+11 dBm	_____dBm
+10 dBm	_____dBm
+ 9 dBm	_____dBm
+ 8 dBm	_____dBm
+ 7 dBm	_____dBm
+ 6 dBm	_____dBm
+ 5 dBm	_____dBm

* Specification is ±1.0 dB.

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+17 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69137A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+17 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (typical, not a specification).

3-11 Power Level Accuracy And Flatness Tests (Continued)
(Model 69037A/69137A with Option 15A High Power & Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz

Set L1 to:	**Measured Power ***
+15 dBm	_____dBm
+14 dBm	_____dBm
+13 dBm	_____dBm
+12 dBm	_____dBm
+11 dBm	_____dBm
+10 dBm	_____dBm
+ 9 dBm	_____dBm
+ 8 dBm	_____dBm
+ 7 dBm	_____dBm
+ 6 dBm	_____dBm
+ 5 dBm	_____dBm
+ 4 dBm	_____dBm
+ 3 dBm	_____dBm

* Specification is ±1.0 dB.

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+15 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69137A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+15 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 6.0 dB (typical, not a specification).

ANRITSU Model 69037A/69137A **Date:** _____

Serial Number _____ **Calibrated By:** _____

4-7 Preliminary Calibration

Procedure Step	**Step Completion**
1. Internal DVM Calibration (calterm119)	_____
2. Fine Loop Pretune DAC Calibration (calterm 136)	_____
3. Sweep Time DAC Calibration (calterm 132)	_____
4. YIG Frequency Offset DAC Calibration (calterm 134)	_____
5. YIG Frequency Linearizer DACs Calibration (calterm 127)	_____
6. 100 MHz Reference Oscillator Calibration (calterm 130)	_____
7. Ramp Center DAC Calibration (calterm 129)	_____
8. Sweep Width DAC Calibration (calterm 133)	_____
9. Center Frequency DAC Calibration (calterm 114)	_____
10. Store the Calibration Data	_____

4-8 Switched Filter Shaper Calibration

Log Amplifier Zero Calibration **Step Completion**

1. Log Amplifier Zero Calibration (calterm 115) . . . . . _____

Limiter DAC Adjustment (69037A/69137A's with Option 15A)

2. Limiter DAC adjustment (calterm 145) . . . . . _____

Shaper DAC Adjustment

2. Shaper DAC Adjustment (calterm 138) . . . . . _____
3. Store the Calibration Data . . . . . _____

4-9 RF Level Calibration

This calibration is performed using an automatic test system. Contact ANRITSU Customer Service for further information.

4-10 ALC Slope Calibration (69137A)

Procedure Step **Step Completion**

5. ALC Slope DAC adjustment . . . . . _____
6. Store the DAC setting value(s). . . . . _____

4-11 ALC Bandwidth Calibration

Procedure Step **Step Completion**

1. ALC Bandwidth Calibration (Calterm 110) . . . . . _____
2. Store the Calibration Data . . . . . _____

4-12 AM Calibration (69137A)

Procedure Step	Step Completion
2. Linear AM Calibration (calterm 112)	_____
3. Log AM Calibration (calterm 113)	_____
4. AM Meter Calibration (calterm 147)	_____
5. Store the Calibration Data	_____

4-13 FM Calibration (69137A)

Procedure Step	Step Completion
1. FM Meter Calibration (calterm 123)	_____
2. FM Variable Gain Linearity Calibration (calterm 148)	_____
3. FM Wide Sensitivity Calibration (calterm 124)	_____
4. FM Narrow Sensitivity Calibration (calterm 125)	_____
5. FM Rear Panel Input Gain Calibration (calterm 149)	_____
6. Store the Calibration Data	_____

ANRITSU Model 69045A/69145A **Date:** _____

Serial Number _____ **Tested By:** _____

3-6 Internal Time Base Aging Rate Test

Test Procedure	Measured Value	Upper Limit
Record frequency error value	_____	
Record frequency error value (after 24 hours)	_____	
Record the computed aging rate	_____per day	$2x10^{-8}$ per day ($5x10^{-10}$ per day with Option 16)

3-7 Frequency Synthesis Tests

Coarse Loop/YIG Loop Test Procedure

Test Frequency (in GHz)	Measured Value *
1.000 000 000	_____
2.000 000 000	_____
3.000 000 000	_____
4.000 000 000	_____
5.000 000 000	_____
6.000 000 000	_____
7.000 000 000	_____
8.000 000 000	_____
9.000 000 000	_____
10.000 000 000	_____
11.000 000 000	_____
12.000 000 000	_____
13.000 000 000	_____
14.000 000 000	_____
15.000 000 000	_____
16.000 000 000	_____
17.000 000 000	_____
18.000 000 000	_____
19.000 000 000	_____
20.000 000 000	_____

* Specification for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (Standard 69X45A)

Test Frequency (in GHz)	Measured Value **
1.000 001 000	_____
1.000 002 000	_____
1.000 003 000	_____
1.000 004 000	_____
1.000 005 000	_____
1.000 006 000	_____
1.000 007 000	_____
1.000 008 000	_____
1.000 009 000	_____
1.000 010 000	_____

** Specifications for all frequencies listed above is ±100 Hz

Fine Loop Test Procedure (69X45A with Option 11)

Test Frequency (in GHz)	Measured Value ***
1.000 000 100	_____
1.000 000 200	_____
1.000 000 300	_____
1.000 000 400	_____
1.000 000 500	_____
1.000 000 600	_____
1.000 000 700	_____
1.000 000 800	_____
1.000 000 900	_____
1.000 001 000	_____

*** Specification for all frequencies listed above is ±10 Hz.

3-8 Spurious Signals Test: RF Output Signals <2.2 GHz

Test Procedure	Measured Value	Upper Limit
Set F1 to 500 MHz Record the level of all harmonics of the 500 MHz carrier		
1.0 GHz (2nd harmonic)	_____dBc	–50 dBc
1.5 GHz (3rd harmonic)	_____dBc	–50 dBc
2.0 GHz (4th harmonic)	_____dBc	–50 dBc
2.5 GHz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 800 MHz Record the level of all harmonics of the 800 MHz carrier		
1.6 GHz (2nd harmonic)	_____dBc	–50 dBc
2.4 GHz (3rd harmonic)	_____dBc	–50 dBc
3.2 GHz (4th harmonic)	_____dBc	–50 dBc
4.0 GHz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 1.3 GHz Record the level of all harmonics of the 1.3 GHz carrier		
2.6 GHz (2nd harmonic)	_____dBc	–50 dBc
3.9 GHz (3rd harmonic)	_____dBc	–50 dBc
5.2 GHz (4th harmonic)	_____dBc	–50 dBc
6.5 GHz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 2.1 GHz Record the level of all harmonics of the 2.1 GHz carrier		
4.2 GHz (2nd harmonic)	_____dBc	–50 dBc
6.3 GHz (3rd harmonic)	_____dBc	–50 dBc
8.2 GHz (4th harmonic)	_____dBc	–50 dBc
10.2 GHz (5th harmonic)	_____dBc	–50 dBc

3-9 Harmonic Test: RF Output Signals From 2.2 to 20 GHz

Test Procedure (2.2 to 10 GHz)	**Measured Value**	**Upper Limit**
Set F1 to 2.4 GHz Record the level of all harmonics of the 2.4 GHz carrier:		
4.8 GHz (2nd harmonic)	_____dBc	–60 dBc*
7.2 GHz (3rd harmonic)	_____dBc	–60 dBc*
9.6 GHz (4th harmonic)	_____dBc	–60 dBc*
12.0 GHz (5th harmonic)	_____dBc	–60 dBc*
14.4 GHz (6th harmonic)	_____dBc	–60 dBc*
16.8 GHz (7th harmonic)	_____dBc	–60 dBc*
19.2 GHz (8th harmonic)	_____dBc	–60 dBc*
Set F1 to 3.6 GHz Record the level of all harmonics of the 3.6 GHz carrier:		
7.2 GHz (2nd harmonic)	_____dBc	–60 dBc*
10.8 GHz (3rd harmonic)	_____dBc	–60 dBc*
14.4 GHz (4th harmonic)	_____dBc	–60 dBc*
18.0 Ghz (5th harmonic)	_____dBc	–60 dBc*
Set F1 to 7.0 GHz Record the level of all harmonics of the 7 GHz carrier:		
14.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 10.0 GHz Record the level of all harmonics of the 10 GHz carrier:		
20.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc if Option 15A (High Power) installed.

3-9 Harmonic Test: RF Output Signals From 2.2 to 20 GHz (Continued)

Test Procedure (11 to 20 GHz)	Measured Value	Upper Limit
Set F1 to 12.4 GHz Record the level of all harmonics of the 12.4 GHz carrier:		
24.8 GHz (2nd harmonic)	_____dBc	–60 dBc*
37.2 GHz (3rd harmonic)	_____dBc	–60 dBc*
Set F1 to 16.0 GHz Record the level of all harmonics of the 16.0 GHz carrier:		
32.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 20.0 GHz Record the level of all harmonics of the 20.0 GHz carrier:		
40.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc if Option 15A (High Power) installed.

3-10 Single Sideband Phase Noise Test

Test Procedure	Measured Value	Upper Limit
Set F1 to 0.6 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–89 dBc
1 kHz	_____dBc	–109 dBc
10 kHz	_____dBc	–109 dBc
100 kHz	_____dBc	–114 dBc
Set F1 to 2.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–83 dBc
1 kHz	_____dBc	–103 dBc
10 kHz	_____dBc	–103 dBc
100 kHz	_____dBc	–108 dBc
Set F1 to 6.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–75 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 10.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–71 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 20.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–63 dBc
1 kHz	_____dBc	–92 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc

3-11 Power Level Accuracy and Flatness Tests (Model 69045A/69145A without Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+13 dBm	_____dBm	+13 dBm	_____dBm
+12 dBm	_____dBm	+12 dBm	_____dBm
+11 dBm	_____dBm	+11 dBm	_____dBm
+10 dBm	_____dBm	+10 dBm	_____dBm
+ 9 dBm	_____dBm	+ 9 dBm	_____dBm
+ 8 dBm	_____dBm	+ 8 dBm	_____dBm
+ 7 dBm	_____dBm	+ 7 dBm	_____dBm
+ 6 dBm	_____dBm	+ 6 dBm	_____dBm
+ 5 dBm	_____dBm	+ 5 dBm	_____dBm
+ 4 dBm	_____dBm	+ 4 dBm	_____dBm
+ 3 dBm	_____dBm	+ 3 dBm	_____dBm
+ 2 dBm	_____dBm	+ 2 dBm	_____dBm
+ 1 dBm	_____dBm	+ 1 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+13 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69145A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+13 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69045A/69145A with Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+11 dBm	_____dBm	+11 dBm	_____dBm
+10 dBm	_____dBm	+10 dBm	_____dBm
+ 9 dBm	_____dBm	+ 9 dBm	_____dBm
+ 8 dBm	_____dBm	+ 8 dBm	_____dBm
+ 7 dBm	_____dBm	+ 7 dBm	_____dBm
+ 6 dBm	_____dBm	+ 6 dBm	_____dBm
+ 5 dBm	_____dBm	+ 5 dBm	_____dBm
+ 4 dBm	_____dBm	+ 4 dBm	_____dBm
+ 3 dBm	_____dBm	+ 3 dBm	_____dBm
+ 2 dBm	_____dBm	+ 2 dBm	_____dBm
+ 1 dBm	_____dBm	+ 1 dBm	_____dBm
+ 0 dBm	_____dBm	+ 0 dBm	_____dBm
– 1 dBm	_____dBm	– 1 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+11 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69145A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+11 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 6.0 dB (typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued)
(Model 69045A/69145A with Option 15A High Power & without Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+13 dBm	_____dBm	+17 dBm	_____dBm
+12 dBm	_____dBm	+16 dBm	_____dBm
+11 dBm	_____dBm	+15 dBm	_____dBm
+10 dBm	_____dBm	+14 dBm	_____dBm
+ 9 dBm	_____dBm	+13 dBm	_____dBm
+ 8 dBm	_____dBm	+ 12dBm	_____dBm
+ 7 dBm	_____dBm	+11 dBm	_____dBm
+ 6 dBm	_____dBm	+10 dBm	_____dBm
+ 5 dBm	_____dBm	+ 9 dBm	_____dBm
+ 4 dBm	_____dBm	+ 8 dBm	_____dBm
+ 3 dBm	_____dBm	+ 7dBm	_____dBm
+ 2 dBm	_____dBm	+ 6 dBm	_____dBm
+ 1 dBm	_____dBm	+ 5 dBm	_____dBm

* Specification is ±1.0 dB.

* Specification is ±1.0 dB.

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+13 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69145A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+13 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69045A/69145A with Option 15A High Power & Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+11 dBm	_____dBm	+15 dBm	_____dBm
+10 dBm	_____dBm	+14 dBm	_____dBm
+ 9 dBm	_____dBm	+13 dBm	_____dBm
+ 8 dBm	_____dBm	+12 dBm	_____dBm
+ 7 dBm	_____dBm	+11 dBm	_____dBm
+ 6 dBm	_____dBm	+10 dBm	_____dBm
+ 5 dBm	_____dBm	+ 9 dBm	_____dBm
+ 4 dBm	_____dBm	+ 8 dBm	_____dBm
+ 3 dBm	_____dBm	+ 7 dBm	_____dBm
+ 2 dBm	_____dBm	+ 6 dBm	_____dBm
+ 1 dBm	_____dBm	+ 5 dBm	_____dBm
+ 0 dBm	_____dBm	+ 4 dBm	_____dBm
– 1 dBm	_____dBm	+ 3 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+11 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69145A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+11 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 6.0 dB (typical, not a specification).

ANRITSU Model 69045A/69145A **Date:** _____

Serial Number _____ **Calibrated By:** _____

4-7 Preliminary Calibration

Procedure Step	**Step Completion**
1. Internal DVM Calibration (calterm119)	_____
2. Fine Loop Pretune DAC Calibration (calterm 136)	_____
3. Sweep Time DAC Calibration (calterm 132)	_____
4. YIG Frequency Offset DAC Calibration (calterm 134)	_____
5. YIG Frequency Linearizer DACs Calibration (calterm 127)	_____
6. 100 MHz Reference Oscillator Calibration (calterm 130)	_____
7. Ramp Center DAC Calibration (calterm 129)	_____
8. Sweep Width DAC Calibration (calterm 133)	_____
9. Center Frequency DAC Calibration (calterm 114)	_____
10. Store the Calibration Data	_____

4-8 Switched Filter Shaper Calibration

Log Amplifier Zero Calibration **Step Completion**

1. Log Amplifier Zero Calibration (calterm 115) . . . . . _____

Limiter DAC Adjustment (68045A/69145A's with Option 15A)

2. Limiter DAC Adjustment (calterm 145). . . . . _____

Shaper DAC Adjustment

2. Shaper DAC Adjustment (calterm 138) . . . . . _____
3. Store the Calibration Data . . . . . _____

4-9 RF Level Calibration

This calibration is performed using an automatic test system. Contact ANRITSU Customer Service for further information.

4-10 ALC Slope Calibration (69145A)

Procedure Step **Step Completion**

5. ALC Slope DAC adjustment . . . . . _____
6. Store the DAC setting value(s). . . . . _____

4-11 ALC Bandwidth Calibration

Procedure Step **Step Completion**

1. ALC Bandwidth Calibration (Calterm 110) . . . . . _____
2. Store the Calibration Data . . . . . _____

4-12 AM Calibration (69145A)

Procedure Step	Step Completion
2. Linear AM Calibration (calterm 112)	_____
3. Log AM Calibration (calterm 113)	_____
4. AM Meter Calibration (calterm 147)	_____
5. Store the Calibration Data	_____

4-13 FM Calibration (69145A)

Procedure Step	Step Completion
1. FM Meter Calibration (calterm 123)	_____
2. FM Variable Gain Linearity Calibration (calterm 148)	_____
3. FM Wide Sensitivity Calibration (calterm 124)	_____
4. FM Narrow Sensitivity Calibration (calterm 125)	_____
5. FM Rear Panel Input Gain Calibration (calterm 149)	_____
6. Store the Calibration Data	_____

ANRITSU Model 69047A/69147A **Date:** _____

Serial Number _____ **Tested By:** _____

3-6 Internal Time Base Aging Rate Test

Test Procedure	**Measured Value**	**Upper Limit**
Record frequency error value	_____	
Record frequency error value (after 24 hours)	_____	
Record the computed aging rate	_____per day	$2x10^{-8}$ per day ($5x10^{-10}$ per day with Option 16)

3-7 Frequency Synthesis Tests

Coarse Loop/YIG Loop Test Procedure

Test Frequency (in GHz)	Measured Value *
1.000 000 000	_____
2.000 000 000	_____
3.000 000 000	_____
4.000 000 000	_____
5.000 000 000	_____
6.000 000 000	_____
7.000 000 000	_____
8.000 000 000	_____
9.000 000 000	_____
10.000 000 000	_____
11.000 000 000	_____
12.000 000 000	_____
13.000 000 000	_____
14.000 000 000	_____
15.000 000 000	_____
16.000 000 000	_____
17.000 000 000	_____
18.000 000 000	_____
19.000 000 000	_____
20.000 000 000	_____

* Specification for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (Standard 69X47A)

Test Frequency (in GHz)	Measured Value **
1.000 001 000	_____
1.000 002 000	_____
1.000 003 000	_____
1.000 004 000	_____
1.000 005 000	_____
1.000 006 000	_____
1.000 007 000	_____
1.000 008 000	_____
1.000 009 000	_____
1.000 010 000	_____

** Specifications for all frequencies listed above is ±100 Hz

Fine Loop Test Procedure (69X47A with Option 11)

Test Frequency (in GHz)	Measured Value ***
1.000 000 100	_____
1.000 000 200	_____
1.000 000 300	_____
1.000 000 400	_____
1.000 000 500	_____
1.000 000 600	_____
1.000 000 700	_____
1.000 000 800	_____
1.000 000 900	_____
1.000 001 000	_____

*** Specification for all frequencies listed above is ±10 Hz.

3-8 Spurious Signals Test: RF Output Signals <2 GHz

Test Procedure	Measured Value	Upper Limit
Set F1 to 10 MHz Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 20 MHz Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 30 MHz Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 40 MHz Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 350 MHz Record the presence of the worst case harmonic	_____dBc	–40 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 1.6 GHz Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 1.6 GHz Record the level of the harmonics of the 1.6 GHz carrier: 3.2 GHz (2nd harmonic)	_____dBc	–40 dBc
4.8 GHz (3rd harmonic)	_____dBc	–40 dBc

3-9 Harmonic Test: RF Output Signals From 2 to 20 GHz

Test Procedure (2 to 10 GHz)	**Measured Value**	**Upper Limit**
Set F1 to 2.1 GHz Record the level of all harmonics of the 2.1 GHz carrier:		
4.2 GHz (2nd harmonic)	_____dBc	–60 dBc*
6.3 GHz (3rd harmonic)	_____dBc	–60 dBc*
8.4 GHz (4th harmonic)	_____dBc	–60 dBc*
10.5 GHz (5th harmonic)	_____dBc	–60 dBc*
12.6 GHz (6th harmonic)	_____dBc	–60 dBc*
14.7 GHz (7th harmonic)	_____dBc	–60 dBc*
16.8 GHz (8th harmonic)	_____dBc	–60 dBc*
18.9 GHz (9th harmonic)	_____dBc	–60 dBc*
Set F1 to 3.6 GHz Record the level of all harmonics of the 3.6 GHz carrier:		
7.2 GHz (2nd harmonic)	_____dBc	–60 dBc*
10.8 GHz (3rd harmonic)	_____dBc	–60 dBc*
14.4 GHz (4th harmonic)	_____dBc	–60 dBc*
18.0 Ghz (5th harmonic)	_____dBc	–60 dBc*
Set F1 to 7.0 GHz Record the level of all harmonics of the 7 GHz carrier:		
14.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 10.0 GHz Record the level of all harmonics of the 10 GHz carrier:		
20.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc if Option 15A (High Power) installed.

3-9 Harmonic Test: RF Output Signals From 2 to 20 GHz (Continued)

Test Procedure (11 to 20 GHz)	Measured Value	Upper Limit
Set F1 to 12.4 GHz Record the level of all harmonics of the 12.4 GHz carrier:		
24.8 GHz (2nd harmonic)	_____dBc	–60 dBc*
37.2 GHz (3rd harmonic)	_____dBc	–60 dBc*
Set F1 to 16.0 GHz Record the level of all harmonics of the 16.0 GHz carrier:		
32.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 20.0 GHz Record the level of all harmonics of the 20.0 GHz carrier:		
40.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc if Option 15A (High Power) installed.

3-10 Single Sideband Phase Noise Test

Test Procedure	Measured Value	Upper Limit
Set F1 to 0.6 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–77 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc
Set F1 to 2.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–77 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 6.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–75 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 10.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–71 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 20.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–63 dBc
1 kHz	_____dBc	–92 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc

3-11 Power Level Accuracy and Flatness Tests (Model 69047A/69147A without Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+13 dBm	_____dBm	+13 dBm	_____dBm
+12 dBm	_____dBm	+12 dBm	_____dBm
+11 dBm	_____dBm	+11 dBm	_____dBm
+10 dBm	_____dBm	+10 dBm	_____dBm
+ 9 dBm	_____dBm	+ 9 dBm	_____dBm
+ 8 dBm	_____dBm	+ 8 dBm	_____dBm
+ 7 dBm	_____dBm	+ 7 dBm	_____dBm
+ 6 dBm	_____dBm	+ 6 dBm	_____dBm
+ 5 dBm	_____dBm	+ 5 dBm	_____dBm
+ 4 dBm	_____dBm	+ 4 dBm	_____dBm
+ 3 dBm	_____dBm	+ 3 dBm	_____dBm
+ 2 dBm	_____dBm	+ 2 dBm	_____dBm
+ 1 dBm	_____dBm	+ 1 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+13 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 1.6 dB (0.05 to 20 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69147A only)

Set L1 to:	Max Power	Min Power	Variation ***
+13 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 2.0 dB (0.05 to 20 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69047A/69147A with Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+11 dBm	_____dBm	+11 dBm	_____dBm
+10 dBm	_____dBm	+10 dBm	_____dBm
+ 9 dBm	_____dBm	+ 9 dBm	_____dBm
+ 8 dBm	_____dBm	+ 8 dBm	_____dBm
+ 7 dBm	_____dBm	+ 7 dBm	_____dBm
+ 6 dBm	_____dBm	+ 6 dBm	_____dBm
+ 5 dBm	_____dBm	+ 5 dBm	_____dBm
+ 4 dBm	_____dBm	+ 4 dBm	_____dBm
+ 3 dBm	_____dBm	+ 3 dBm	_____dBm
+ 2 dBm	_____dBm	+ 2 dBm	_____dBm
+ 1 dBm	_____dBm	+ 1 dBm	_____dBm
+ 0 dBm	_____dBm	+ 0 dBm	_____dBm
– 1 dBm	_____dBm	– 1 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+11 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 1.6 dB (0.05 to 20 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69147A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+11 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 7.0 dB (0.01 to 0.05 GHz); 6.0 dB (0.05 to 20 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69047A/69147A with Option 15A High Power & without Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+13 dBm	_____dBm	+17 dBm	_____dBm
+12 dBm	_____dBm	+16 dBm	_____dBm
+11 dBm	_____dBm	+15 dBm	_____dBm
+10 dBm	_____dBm	+14 dBm	_____dBm
+ 9 dBm	_____dBm	+13 dBm	_____dBm
+ 8 dBm	_____dBm	+ 12dBm	_____dBm
+ 7 dBm	_____dBm	+11 dBm	_____dBm
+ 6 dBm	_____dBm	+10 dBm	_____dBm
+ 5 dBm	_____dBm	+ 9 dBm	_____dBm
+ 4 dBm	_____dBm	+ 8 dBm	_____dBm
+ 3 dBm	_____dBm	+ 7dBm	_____dBm
+ 2 dBm	_____dBm	+ 6 dBm	_____dBm
+ 1 dBm	_____dBm	+ 5 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+13 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 1.6 dB (0.05 to 20 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69147A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+13 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 2.0 dB (0.05 to 20 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued)
(Model 69047A/69147A with Option 15A High Power & Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+11 dBm	_____dBm	+15 dBm	_____dBm
+10 dBm	_____dBm	+14 dBm	_____dBm
+ 9 dBm	_____dBm	+13 dBm	_____dBm
+ 8 dBm	_____dBm	+12 dBm	_____dBm
+ 7 dBm	_____dBm	+11 dBm	_____dBm
+ 6 dBm	_____dBm	+10 dBm	_____dBm
+ 5 dBm	_____dBm	+ 9 dBm	_____dBm
+ 4 dBm	_____dBm	+ 8 dBm	_____dBm
+ 3 dBm	_____dBm	+ 7 dBm	_____dBm
+ 2 dBm	_____dBm	+ 6 dBm	_____dBm
+ 1 dBm	_____dBm	+ 5 dBm	_____dBm
+ 0 dBm	_____dBm	+ 4 dBm	_____dBm
– 1 dBm	_____dBm	+ 3 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+11 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 1.6 dB (0.05 to 20 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69147A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+11 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 7.0 dB (0.01 to 0.05 GHz); 6.0 dB (0.05 to 20 GHz)(typical, not a specification).

ANRITSU Model 69047A/69147A **Date:** _____

Serial Number _____ **Calibrated By:** _____

4-7 Preliminary Calibration

Procedure Step	**Step Completion**
1. Internal DVM Calibration (calterm119)	_____
2. Fine Loop Pretune DAC Calibration (calterm 136)	_____
3. Sweep Time DAC Calibration (calterm 132)	_____
4. YIG Frequency Offset DAC Calibration (calterm 134)	_____
5. YIG Frequency Linearizer DACs Calibration (calterm 127)	_____
6. 100 MHz Reference Oscillator Calibration (calterm 130)	_____
7. Ramp Center DAC Calibration (calterm 129)	_____
8. Sweep Width DAC Calibration (calterm 133)	_____
9. Center Frequency DAC Calibration (calterm 114)	_____
10. Store the Calibration Data	_____

4-8 Switched Filter Shaper Calibration

Log Amplifier Zero Calibration **Step Completion**

1. Log Amplifier Zero Calibration (calterm 115) . . . . . _____

Limiter DAC Adjustment (69047A/69147A's with Option 15A)

2. Limiter DAC Adjustment (calterm 145). . . . . _____

Shaper DAC Adjustment

2. Shaper DAC Adjustment (calterm 138) . . . . . _____
3. Store the Calibration Data . . . . . _____

4-9 RF Level Calibration

This calibration is performed using an automatic test system. Contact ANRITSU Customer Service for further information.

4-10 ALC Slope Calibration (69147A)

Procedure Step **Step Completion**

5. ALC Slope DAC adjustment . . . . . _____
6. Store the DAC setting value(s). . . . . _____

4-11 ALC Bandwidth Calibration

Procedure Step **Step Completion**

1. ALC Bandwidth Calibration (Calterm 110) . . . . . _____
2. Store the Calibration Data . . . . . _____

4-12 AM Calibration (69147A)

Procedure Step	Step Completion
2. Linear AM Calibration (calterm 112)	_____
3. Log AM Calibration (calterm 113)	_____
4. AM Meter Calibration (calterm 147)	_____
5. Store the Calibration Data	_____

4-13 FM Calibration (69147A)

Procedure Step	Step Completion
1. FM Meter Calibration (calterm 123)	_____
2. FM Variable Gain Linearity Calibration (calterm 148)	_____
3. FM Wide Sensitivity Calibration (calterm 124)	_____
4. FM Narrow Sensitivity Calibration (calterm 125)	_____
5. FM Rear Panel Input Gain Calibration (calterm 149)	_____
6. Store the Calibration Data	_____

ANRITSU Model 69053A/69153A **Date:** _____

Serial Number _____ **Tested By:** _____

3-6 Internal Time Base Aging Rate Test

Test Procedure	**Measured Value**	**Upper Limit**
Record frequency error value	_____	
Record frequency error value (after 24 hours)	_____	
Record the computed aging rate	_____per day	$2x10^{-8}$ per day ($5x10^{-10}$ per day with Option 16)

3-7 Frequency Synthesis Tests

Coarse Loop/YIG Loop Test Procedure

Test Frequency (in GHz)	Measured Value *	Test Frequency (in GHz)	Measured Value *
2.000 000 000	_____	21.000 000 000	_____
3.000 000 000	_____	22.000 000 000	_____
4.000 000 000	_____	23.000 000 000	_____
5.000 000 000	_____	24.000 000 000	_____
6.000 000 000	_____	25.000 000 000	_____
7.000 000 000	_____	26.000 000 000	_____
8.000 000 000	_____		
9.000 000 000	_____		
10.000 000 000	_____		
11.000 000 000	_____		
12.000 000 000	_____		
13.000 000 000	_____		
14.000 000 000	_____		
15.000 000 000	_____		
16.000 000 000	_____		
17.000 000 000	_____		
18.000 000 000	_____		
19.000 000 000	_____		
20.000 000 000	_____		

* Specification for all frequencies listed above is ±100 Hz.

3-7 Frequency Synthesis Tests (Continued)

Fine Loop Test Procedure (Standard 69X53A)

Test Frequency (in GHz)	Measured Value **
2.000 001 000	_____
2.000 002 000	_____
2.000 003 000	_____
2.000 004 000	_____
2.000 005 000	_____
2.000 006 000	_____
2.000 007 000	_____
2.000 008 000	_____
2.000 009 000	_____
2.000 010 000	_____

** Specification for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (69X53A with Option 11)

Test Frequency (in GHz)	Measured Value ***
2.000 000 100	_____
2.000 000 200	_____
2.000 000 300	_____
2.000 000 400	_____
2.000 000 500	_____
2.000 000 600	_____
2.000 000 700	_____
2.000 000 800	_____
2.000 000 900	_____
2.000 001 000	_____

*** Specification for all frequencies listed above is ±10 Hz.

3-8 Spurious Signals Test: RF Output Signals <2 GHz

This test is not applicable to the 69053A/69153A model.

3-9 Harmonic Test: RF Output Signals From 2 to 20 GHz

Test Procedure (2 to 10 GHz)	Measured Value	Upper Limit
Set F1 to 2.1 GHz		
Record the level of all harmonics of the 2.1 GHz carrier:		
4.2 GHz (2nd harmonic)	_____dBc	–60 dBc*
6.3 GHz (3rd harmonic)	_____dBc	–60 dBc*
8.4 GHz (4th harmonic)	_____dBc	–60 dBc*
10.5 GHz (5th harmonic)	_____dBc	–60 dBc*
12.6 GHz (6th harmonic)	_____dBc	–60 dBc*
14.7 GHz (7th harmonic)	_____dBc	–60 dBc*
16.8 GHz (8th harmonic)	_____dBc	–60 dBc*
18.9 GHz (9th harmonic)	_____dBc	–60 dBc*
Set F1 to 3.6 GHz		
Record the level of all harmonics of the 3.6 GHz carrier:		
7.2 GHz (2nd harmonic)	_____dBc	–60 dBc*
10.8 GHz (3rd harmonic)	_____dBc	–60 dBc*
14.4 GHz (4th harmonic)	_____dBc	–60 dBc*
18.0 Ghz (5th harmonic)	_____dBc	–60 dBc*
Set F1 to 7.0 GHz		
Record the level of all harmonics of the 7 GHz carrier:		
14.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 10.0 GHz		
Record the level of all harmonics of the 10 GHz carrier:		
20.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc if Option 15A (High Power) installed.

3-9 Harmonic Test: RF Output Signals From 2 to 20 GHz (Continued)

Test Procedure (11 to 20 GHz)	**Measured Value**	**Upper Limit**
Set F1 to 12.4 GHz Record the level of all harmonics of the 12.4 GHz carrier:		
24.8 GHz (2nd harmonic)	_____dBc	–60 dBc*
37.2 GHz (3rd harmonic)	_____dBc	–60 dBc*
Set F1 to 16.0 GHz Record the level of all harmonics of the 16.0 GHz carrier:		
32.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 20.0 GHz Record the level of all harmonics of the 20.0 GHz carrier:		
40.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc if Option 15A (High Power) installed.

3-10 Single Sideband Phase Noise Test

Test Procedure	Measured Value	Upper Limit
Set F1 to 2.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–77 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 6.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–75 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 10.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–71 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 20.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–63 dBc
1 kHz	_____dBc	–92 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc
Set F1 to 26.5 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–60 dBc
1 kHz	_____dBc	–88 dBc
10 kHz	_____dBc	–91 dBc
100 kHz	_____dBc	–93 dBc

3-11 Power Level Accuracy and Flatness Tests (Model 69053A/69153A without Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz		Set F1 to 22.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+ 9 dBm	_____dBm	+ 6 dBm	_____dBm
+ 8 dBm	_____dBm	+ 5 dBm	_____dBm
+ 7 dBm	_____dBm	+ 4 dBm	_____dBm
+ 6 dBm	_____dBm	+ 3 dBm	_____dBm
+ 5 dBm	_____dBm	+ 2 dBm	_____dBm
+ 4 dBm	_____dBm	+ 1 dBm	_____dBm
+ 3 dBm	_____dBm	+ 0 dBm	_____dBm
+ 2 dBm	_____dBm	– 1 dBm	_____dBm
+ 1 dBm	_____dBm	– 2 dBm	_____dBm
+ 0 dBm	_____dBm	– 3 dBm	_____dBm
– 1 dBm	_____dBm	– 4 dBm	_____dBm
– 2 dBm	_____dBm	– 5 dBm	_____dBm
– 3 dBm	_____dBm	– 6 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+ 6 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69153A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+ 6 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (2 to 20 GHz); 4.0 dB (20 to 26.5 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69053A/69153A with Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz		Set F1 to 22.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+ 7 dBm	_____dBm	+ 3.5 dBm	_____dBm
+ 6 dBm	_____dBm	+ 2.5 dBm	_____dBm
+ 5 dBm	_____dBm	+ 1.5 dBm	_____dBm
+ 4 dBm	_____dBm	+ 0.5 dBm	_____dBm
+ 3 dBm	_____dBm	– 0.5 dBm	_____dBm
+ 2 dBm	_____dBm	– 1.5 dBm	_____dBm
+ 1 dBm	_____dBm	– 2.5 dBm	_____dBm
+ 0 dBm	_____dBm	– 3.5 dBm	_____dBm
– 1 dBm	_____dBm	– 4.5 dBm	_____dBm
– 2 dBm	_____dBm	– 5.5 dBm	_____dBm
– 3 dBm	_____dBm	– 6.5 dBm	_____dBm
– 4 dBm	_____dBm	– 7.5 dBm	_____dBm
– 5 dBm	_____dBm	– 8.5 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+ 3.5 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69153A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+ 3.5 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 6.0 dB (2 to 20 GHz); 8.2 dB (20 to 26.5 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69053A/69153A with Option 15A High Power & without Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz		Set F1 to 22.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+13 dBm	_____dBm	+10 dBm	_____dBm
+12 dBm	_____dBm	+ 9 dBm	_____dBm
+11 dBm	_____dBm	+ 8 dBm	_____dBm
+10 dBm	_____dBm	+ 7 dBm	_____dBm
+ 9 dBm	_____dBm	+ 6 dBm	_____dBm
+ 8 dBm	_____dBm	+ 5 dBm	_____dBm
+ 7 dBm	_____dBm	+ 4 dBm	_____dBm
+ 6 dBm	_____dBm	+ 3 dBm	_____dBm
+ 5 dBm	_____dBm	+ 2 dBm	_____dBm
+ 4 dBm	_____dBm	+ 1 dBm	_____dBm
+ 3 dBm	_____dBm	+ 0 dBm	_____dBm
+ 2 dBm	_____dBm	– 1 dBm	_____dBm
+ 1 dBm	_____dBm	– 2 dBm	_____dBm

* Specification is ±1.0 dB.

* Specification is ±1.0 dB.

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+ 10 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69153A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+ 10 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (2 to 20 GHz); 4.0 dB (20 to 26.5 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69053A/69153A with Option 15A High Power & Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz		Set F1 to 22.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+11 dBm	_____dBm	+ 7.5 dBm	_____dBm
+10 dBm	_____dBm	+ 6.5 dBm	_____dBm
+ 9 dBm	_____dBm	+ 5.5 dBm	_____dBm
+ 8 dBm	_____dBm	+ 4.5 dBm	_____dBm
+ 7 dBm	_____dBm	+ 3.5 dBm	_____dBm
+ 6 dBm	_____dBm	+ 2.5 dBm	_____dBm
+ 5 dBm	_____dBm	+ 1.5 dBm	_____dBm
+ 4 dBm	_____dBm	+ 0.5 dBm	_____dBm
+ 3 dBm	_____dBm	– 0.5 dBm	_____dBm
+ 2 dBm	_____dBm	– 1.5 dBm	_____dBm
+ 1 dBm	_____dBm	– 2.5 dBm	_____dBm
+ 0 dBm	_____dBm	– 3.5 dBm	_____dBm
– 1 dBm	_____dBm	– 4.5 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+ 7.5 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69153A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+ 7.5 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 6.0 dB (2 to 20 GHz); 8.2 dB (20 to 26.5 GHz)(typical, not a specification).

ANRITSU Model 69053A/69153A **Date:** _____

Serial Number _____ **Calibrated By:** _____

4-7 Preliminary Calibration

Procedure Step	**Step Completion**
1. Internal DVM Calibration (calterm119)	_____
2. Fine Loop Pretune DAC Calibration (calterm 136)	_____
3. Sweep Time DAC Calibration (calterm 132)	_____
4. YIG Frequency Offset DAC Calibration (calterm 134)	_____
5. YIG Frequency Linearizer DACs Calibration (calterm 127)	_____
6. 100 MHz Reference Oscillator Calibration (calterm 130)	_____
7. Ramp Center DAC Calibration (calterm 129)	_____
8. Sweep Width DAC Calibration (calterm 133)	_____
9. Center Frequency DAC Calibration (calterm 114)	_____
10. Store the Calibration Data	_____

4-8 Switched Filter Shaper Calibration

Log Amplifier Zero Calibration **Step Completion**

1. Log Amplifier Zero Calibration (calterm 115) . . . . . _____

Limiter DAC Adjustment (69053A/69153A with Option 15A)

2. Limiter DAC Adjustment (calterm 145). . . . . _____

Shaper DAC Adjustment

2. Shaper DAC Adjustment (calterm 138) . . . . . _____
3. Store the Calibration Data . . . . . _____

4-9 RF Level Calibration

This calibration is performed using an automatic test system. Contact ANRITSU Customer Service for further information.

4-10 ALC Slope Calibration (69153A)

Procedure Step **Step Completion**

5. ALC Slope DAC adjustment . . . . . _____
6. Store the DAC setting value(s). . . . . _____

4-11 ALC Bandwidth Calibration

Procedure Step **Step Completion**

1. ALC Bandwidth Calibration (Calterm 110) . . . . . _____
2. Store the Calibration Data . . . . . _____

4-12 AM Calibration (69153A)

Procedure Step	Step Completion
2. Linear AM Calibration (calterm 112)	_____
3. Log AM Calibration (calterm 113)	_____
4. AM Meter Calibration (calterm 147)	_____
5. Store the Calibration Data	_____

4-13 FM Calibration (69153A)

Procedure Step	Step Completion
1. FM Meter Calibration (calterm 123)	_____
2. FM Variable Gain LInearity Calibration (calterm 148)	_____
3. FM Wide Sensitivity Calibration (calterm 124)	_____
4. FM Narrow Sensitivity Calibratioin (calterm 125)	_____
5. FM Rear Panel Input Gain Calibration (calterm 149)	_____
6. Store the Calibration Data	_____

ANRITSU Model 69055A/69155A **Date:** _____

Serial Number _____ **Tested By:** _____

3-6 Internal Time Base Aging Rate Test

Test Procedure	**Measured Value**	**Upper Limit**
Record frequency error value	_____	
Record frequency error value (after 24 hours)	_____	
Record the computed aging rate	_____per day	$2x10^{-8}$ per day ($5x10^{-10}$ per day with Option 16)

3-7 Frequency Synthesis Tests

Coarse Loop/YIG Loop Test Procedure

Test Frequency (in GHz)	Measured Value *	Test Frequency (in GHz)	Measured Value *
1.000 000 000	_____	21.000 000 000	_____
2.000 000 000	_____	22.000 000 000	_____
3.000 000 000	_____	23.000 000 000	_____
4.000 000 000	_____	24.000 000 000	_____
5.000 000 000	_____	25.000 000 000	_____
6.000 000 000	_____	26.000 000 000	_____
7.000 000 000	_____		
8.000 000 000	_____		
9.000 000 000	_____		
10.000 000 000	_____		
11.000 000 000	_____		
12.000 000 000	_____		
13.000 000 000	_____		
14.000 000 000	_____		
15.000 000 000	_____		
16.000 000 000	_____		
17.000 000 000	_____		
18.000 000 000	_____		
19.000 000 000	_____		
20.000 000 000	_____		

* Specification for all frequencies listed above is ±100 Hz.

3-7 Frequency Synthesis Tests (Continued)

Fine Loop Test Procedure (Standard 69X55A)

Test Frequency (in GHz)	Measured Value **
1.000 001 000	_____
1.000 002 000	_____
1.000 003 000	_____
1.000 004 000	_____
1.000 005 000	_____
1.000 006 000	_____
1.000 007 000	_____
1.000 008 000	_____
1.000 009 000	_____
1.000 010 000	_____

** Specifications for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (69X55A with Option 11)

Test Frequency (in GHz)	Measured Value ***
1.000 000 100	_____
1.000 000 200	_____
1.000 000 300	_____
1.000 000 400	_____
1.000 000 500	_____
1.000 000 600	_____
1.000 000 700	_____
1.000 000 800	_____
1.000 000 900	_____
1.000 001 000	_____

*** Specification for all frequencies listed above is ±10 Hz.

3-8 Spurious Signals Test: RF Output Signals <2.2 GHz

Test Procedure	Measured Value	Upper Limit
Set F1 to 500 MHz Record the level of all harmonics of the 500 MHz carrier		
1.0 GHz (2nd harmonic)	_____dBc	–50 dBc
1.5 GHz (3rd harmonic)	_____dBc	–50 dBc
2.0 GHz (4th harmonic)	_____dBc	–50 dBc
2.5 GHz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 800 MHz Record the level of all harmonics of the 800 MHz carrier		
1.6 GHz (2nd harmonic)	_____dBc	–50 dBc
2.4 GHz (3rd harmonic)	_____dBc	–50 dBc
3.2 GHz (4th harmonic)	_____dBc	–50 dBc
4.0 GHz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 1.3 GHz Record the level of all harmonics of the 1.3 GHz carrier		
2.6 GHz (2nd harmonic)	_____dBc	–50 dBc
3.9 GHz (3rd harmonic)	_____dBc	–50 dBc
5.2 GHz (4th harmonic)	_____dBc	–50 dBc
6.5 GHz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 2.1 GHz Record the level of all harmonics of the 2.1 GHz carrier		
4.2 GHz (2nd harmonic)	_____dBc	–50 dBc
6.3 GHz (3rd harmonic)	_____dBc	–50 dBc
8.2 GHz (4th harmonic)	_____dBc	–50 dBc
10.2 GHz (5th harmonic)	_____dBc	–50 dBc

3-9 Harmonic Test: RF Output Signals From 2.2 to 20 GHz

Test Procedure (2.2 to 10 GHz)	**Measure Value**	**Upper Limit**
Set F1 to 2.4 GHz Record the level of all harmonics of the 2.4 GHz carrier:		
4.8 GHz (2nd harmonic)	_____dBc	–60 dBc*
7.2 GHz (3rd harmonic)	_____dBc	–60 dBc*
9.6 GHz (4th harmonic)	_____dBc	–60 dBc*
12.0 GHz (5th harmonic)	_____dBc	–60 dBc*
14.4 GHz (6th harmonic)	_____dBc	–60 dBc*
16.8 GHz (7th harmonic)	_____dBc	–60 dBc*
19.2 GHz (8th harmonic)	_____dBc	–60 dBc*
Set F1 to 3.6 GHz Record the level of all harmonics of the 3.6 GHz carrier:		
7.2 GHz (2nd harmonic)	_____dBc	–60 dBc*
10.8 GHz (3rd harmonic)	_____dBc	–60 dBc*
14.4 GHz (4th harmonic)	_____dBc	–60 dBc*
18.0 Ghz (5th harmonic)	_____dBc	–60 dBc*
Set F1 to 7.0 GHz Record the level of all harmonics of the 7 GHz carrier:		
14.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 10.0 GHz Record the level of all harmonics of the 10 GHz carrier:		
20.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc if Option 15A (High Power) installed.

3-9 Harmonic Test: RF Output Signals From 2.2 to 20 GHz (Continued)

Test Procedure (11 to 20 GHz)	Measure Value	Upper Limit
Set F1 to 12.4 GHz		
Record the level of all harmonics of the 12.4 GHz carrier:		
24.8 GHz (2nd harmonic)	_____dBc	–60 dBc*
37.2 GHz (3rd harmonic)	_____dBc	–60 dBc*
Set F1 to 16.0 GHz		
Record the level of all harmonics of the 16.0 GHz carrier:		
32.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 20.0 GHz		
Record the level of all harmonics of the 20.0 GHz carrier:		
40.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc if Option 15A (High Power) installed.

3-10 Single Sideband Phase Noise Test

Test Procedure	Measured Value	Upper Limit
Set F1 to 0.6 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–89 dBc
1 kHz	_____dBc	–109 dBc
10 kHz	_____dBc	–109 dBc
100 kHz	_____dBc	–114 dBc
Set F1 to 2.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–83 dBc
1 kHz	_____dBc	–103 dBc
10 kHz	_____dBc	–103 dBc
100 kHz	_____dBc	–108 dBc

3-10 Single Sideband Phase Noise Test (Continued)

Test Procedure	Measured Value	Upper Limit
Set F1 to 6.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–75 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 10.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–71 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 20.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–63 dBc
1 kHz	_____dBc	–92 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc
Set F1 to 26.5 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–60 dBc
1 kHz	_____dBc	–88 dBc
10 kHz	_____dBc	–91 dBc
100 kHz	_____dBc	–93 dBc

3-11 Power Level Accuracy and Flatness Tests (Model 69055A/69155A without Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz		Set F1 to 22.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+13 dBm	_____dBm	+ 9 dBm	_____dBm	+ 6 dBm	_____dBm
+12 dBm	_____dBm	+ 8 dBm	_____dBm	+ 5 dBm	_____dBm
+11 dBm	_____dBm	+ 7 dBm	_____dBm	+ 4 dBm	_____dBm
+10 dBm	_____dBm	+ 6 dBm	_____dBm	+ 3 dBm	_____dBm
+ 9 dBm	_____dBm	+ 5 dBm	_____dBm	+ 2 dBm	_____dBm
+ 8 dBm	_____dBm	+ 4 dBm	_____dBm	+ 1 dBm	_____dBm
+ 7 dBm	_____dBm	+ 3 dBm	_____dBm	+ 0 dBm	_____dBm
+ 6 dBm	_____dBm	+ 2 dBm	_____dBm	– 1 dBm	_____dBm
+ 5 dBm	_____dBm	+ 1 dBm	_____dBm	– 2 dBm	_____dBm
+ 4 dBm	_____dBm	+ 0 dBm	_____dBm	– 3 dBm	_____dBm
+ 3 dBm	_____dBm	– 1 dBm	_____dBm	– 4 dBm	_____dBm
+ 2 dBm	_____dBm	– 2 dBm	_____dBm	– 5 dBm	_____dBm
+ 1 dBm	_____dBm	– 3 dBm	_____dBm	– 6 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+ 6 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69155A only)

Set L1 to:	Max Power	Min Power	Variation ***
+ 6 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (0.5 to 20 GHz); 4.0 dB (20 to 26.5 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69055A/69155A with Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz		Set F1 to 22.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+11 dBm	_____dBm	+ 7 dBm	_____dBm	+ 3.5 dBm	_____dBm
+10 dBm	_____dBm	+ 6 dBm	_____dBm	+ 2.5 dBm	_____dBm
+ 9 dBm	_____dBm	+ 5 dBm	_____dBm	+ 1.5 dBm	_____dBm
+ 8 dBm	_____dBm	+ 4 dBm	_____dBm	+ 0.5 dBm	_____dBm
+ 7 dBm	_____dBm	+ 3 dBm	_____dBm	– 0.5 dBm	_____dBm
+ 6 dBm	_____dBm	+ 2 dBm	_____dBm	– 1.5 dBm	_____dBm
+ 5 dBm	_____dBm	+ 1 dBm	_____dBm	– 2.5 dBm	_____dBm
+ 4 dBm	_____dBm	+ 0 dBm	_____dBm	– 3.5 dBm	_____dBm
+ 3 dBm	_____dBm	– 1 dBm	_____dBm	– 4.5 dBm	_____dBm
+ 2 dBm	_____dBm	– 2 dBm	_____dBm	– 5.5 dBm	_____dBm
+ 1 dBm	_____dBm	– 3 dBm	_____dBm	– 6.5 dBm	_____dBm
+ 0 dBm	_____dBm	– 4 dBm	_____dBm	– 7.5 dBm	_____dBm
– 1 dBm	_____dBm	– 5 dBm	_____dBm	– 8.5 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+ 3.5 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69155A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+ 3.5 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 6.0 dB (0.5 to 20 GHz); 8.2 dB (20 to 26.5 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued)
(Model 69055A/69155A with Option 15A High Power & without Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz		Set F1 to 22.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+13 dBm	_____dBm	+13 dBm	_____dBm	+10 dBm	_____dBm
+12 dBm	_____dBm	+12 dBm	_____dBm	+ 9 dBm	_____dBm
+11 dBm	_____dBm	+11 dBm	_____dBm	+ 8 dBm	_____dBm
+10 dBm	_____dBm	+10 dBm	_____dBm	+ 7 dBm	_____dBm
+ 9 dBm	_____dBm	+ 9 dBm	_____dBm	+ 6 dBm	_____dBm
+ 8 dBm	_____dBm	+ 8 dBm	_____dBm	+ 5 dBm	_____dBm
+ 7 dBm	_____dBm	+ 7 dBm	_____dBm	+ 4 dBm	_____dBm
+ 6 dBm	_____dBm	+ 6 dBm	_____dBm	+ 3 dBm	_____dBm
+ 5 dBm	_____dBm	+ 5 dBm	_____dBm	+ 2 dBm	_____dBm
+ 4 dBm	_____dBm	+ 4 dBm	_____dBm	+ 1 dBm	_____dBm
+ 3 dBm	_____dBm	+ 3 dBm	_____dBm	+ 0 dBm	_____dBm
+ 2 dBm	_____dBm	+ 2 dBm	_____dBm	– 1 dBm	_____dBm
+ 1 dBm	_____dBm	+ 1 dBm	_____dBm	– 2 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+ 10 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69155A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+ 10 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (0.5 to 20 GHz); 4.0 dB (20 to 26.5 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69055A/69155A with Option 15A High Power & Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz		Set F1 to 22.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+11 dBm	_____dBm	+11 dBm	_____dBm	+ 7.5 dBm	_____dBm
+10 dBm	_____dBm	+10 dBm	_____dBm	+ 6.5 dBm	_____dBm
+ 9 dBm	_____dBm	+ 9 dBm	_____dBm	+ 5.5 dBm	_____dBm
+ 8 dBm	_____dBm	+ 8 dBm	_____dBm	+ 4.5 dBm	_____dBm
+ 7 dBm	_____dBm	+ 7 dBm	_____dBm	+ 3.5 dBm	_____dBm
+ 6 dBm	_____dBm	+ 6 dBm	_____dBm	+ 2.5 dBm	_____dBm
+ 5 dBm	_____dBm	+ 5 dBm	_____dBm	+ 1.5 dBm	_____dBm
+ 4 dBm	_____dBm	+ 4 dBm	_____dBm	+ 0.5 dBm	_____dBm
+ 3 dBm	_____dBm	+ 3 dBm	_____dBm	– 0.5 dBm	_____dBm
+ 2 dBm	_____dBm	+ 2 dBm	_____dBm	– 1.5 dBm	_____dBm
+ 1 dBm	_____dBm	+ 1 dBm	_____dBm	– 2.5 dBm	_____dBm
+ 0 dBm	_____dBm	+ 0 dBm	_____dBm	– 3.5 dBm	_____dBm
– 1 dBm	_____dBm	– 1 dBm	_____dBm	– 4.5 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+ 7.5 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69155A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+ 7.5 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 6.0 dB (0.5 to 20 GHz); 8.2 dB (20 to 26.5 GHz)(typical, not a specification).

ANRITSU Model 69055A/69155A **Date:** _____

Serial Number _____ **Calibrated By:** _____

4-7 Preliminary Calibration

Procedure Step	**Step Completion**
1. Internal DVM Calibration (calterm119)	_____
2. Fine Loop Pretune DAC Calibration (calterm 136)	_____
3. Sweep Time DAC Calibration (calterm 132)	_____
4. YIG Frequency Offset DAC Calibration (calterm 134)	_____
5. YIG Frequency Linearizer DACs Calibration (calterm 127)	_____
6. 100 MHz Reference Oscillator Calibration (calterm 130)	_____
7. Ramp Center DAC Calibration (calterm 129)	_____
8. Sweep Width DAC Calibration (calterm 133)	_____
9. Center Frequency DAC Calibration (calterm 114)	_____
10. Store the Calibration Data	_____

4-8 Switched Filter Shaper Calibration

Log Amplifier Zero Calibration **Step Completion**

1. Log Amplifier Zero Calibration (calterm 115) . . . . . _____

Limiter DAC Adjustment (69055A/69155A with Option 15A)

2. Limiter DAC Adjustment (calterm 145). . . . . _____

Shaper DAC Adjustment

2. Shaper DAC Adjustment (calterm 138) . . . . . _____
3. Store the Calibration Data . . . . . _____

4-9 RF Level Calibration

This calibration is performed using an automatic test system. Contact ANRITSU Customer Service for further information.

4-10 ALC Slope Calibration (69155A)

Procedure Step **Step Completion**

5. ALC Slope DAC adjustment . . . . . _____
6. Store the DAC setting value(s). . . . . _____

4-11 ALC Bandwidth Calibration

Procedure Step **Step Completion**

1. ALC Bandwidth Calibration (Calterm 110) . . . . . _____
2. Store the Calbration Data . . . . . _____

4-12 AM Calibration (69155A)

Procedure Step	Step Completion
2. Linear AM Calibration (calterm 112)	_____
3. Log AM Calibration (calterm 113)	_____
4. AM Meter Calibration (calterm 147)	_____
5. Store the Calibration Data	_____

4-13 FM Calibration (69155A)

Procedure Step	Step Completion
1. FM Meter Calibration (calterm 123)	_____
2. FM Variable Gain Linearity Calibration (calterm 148)	_____
3. FM Wide Calibration (calterm 124)	_____
4. FM Narrow Calibration (calterm 125)	_____
5. FM Rear Panel Input Gain Calibration (calterm 149)	_____
6. Store the Calibration Data	_____

ANRITSU Model 69059A/69159A **Date:** _____

Serial Number _____ **Tested By:** _____

3-6 Internal Time Base Aging Rate Test

Test Procedure	**Measured Value**	**Upper Limit**
Record frequency error value	_____	
Record frequency error value (after 24 hours)	_____	
Record the computed aging rate	_____per day	$2x10^{-8}$ per day ($5x10^{-10}$ per day with Option 16)

3-7 Frequency Synthesis Tests

Coarse Loop/YIG Loop Test Procedure

Test Frequency (in GHz)	Measured Value *	Test Frequency (in GHz)	Measured Value *
1.000 000 000	_____	21.000 000 000	_____
2.000 000 000	_____	22.000 000 000	_____
3.000 000 000	_____	23.000 000 000	_____
4.000 000 000	_____	24.000 000 000	_____
5.000 000 000	_____	25.000 000 000	_____
6.000 000 000	_____	26.000 000 000	_____
7.000 000 000	_____		
8.000 000 000	_____		
9.000 000 000	_____		
10.000 000 000	_____		
11.000 000 000	_____		
12.000 000 000	_____		
13.000 000 000	_____		
14.000 000 000	_____		
15.000 000 000	_____		
16.000 000 000	_____		
17.000 000 000	_____		
18.000 000 000	_____		
19.000 000 000	_____		
20.000 000 000	_____		

* Specification for all frequencies listed above is ±100 Hz.

3-7 Frequency Synthesis Tests (Continued)

Fine Loop Test Procedure (Standard 69X59A)

Test Frequency (in GHz)	Measured Value **
1.000 001 000	_____
1.000 002 000	_____
1.000 003 000	_____
1.000 004 000	_____
1.000 005 000	_____
1.000 006 000	_____
1.000 007 000	_____
1.000 008 000	_____
1.000 009 000	_____
1.000 010 000	_____

** Specifications for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (69X59A with Option 11)

Test Frequency (in GHz)	Measured Value ***
1.000 000 100	_____
1.000 000 200	_____
1.000 000 300	_____
1.000 000 400	_____
1.000 000 500	_____
1.000 000 600	_____
1.000 000 700	_____
1.000 000 800	_____
1.000 000 900	_____
1.000 001 000	_____

*** Specification for all frequencies listed above is ±10 Hz.

3-8 Spurious Signals Test: RF Output Signals <2 GHz

Test Procedure	Measured Value	Upper Limit
Set F1 to 10 MHz		
Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 20 MHz		
Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 30 MHz		
Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 40 MHz		
Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 350 MHz		
Record the presence of the worst case harmonic	_____dBc	–40 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 1.6 GHz		
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 1.6 GHz		
Record the level of the harmonics of the 1.6 GHz carrier:		
3.2 GHz (2nd harmonic)	_____dBc	–40 dBc
4.8 GHz (3rd harmonic)	_____dBc	–40 dBc

3-9 Harmonic Test: RF Output Signals From 2 to 20 GHz

Test Procedure (2 to 10 GHz)	**Measure Value**	**Upper Limit**
Set F1 to 2.1 GHz Record the level of all harmonics of the 2.1 GHz carrier:		
4.2 GHz (2nd harmonic)	_____dBc	–60 dBc*
6.3 GHz (3rd harmonic)	_____dBc	–60 dBc*
8.4 GHz (4th harmonic)	_____dBc	–60 dBc*
10.5 GHz (5th harmonic)	_____dBc	–60 dBc*
12.6 GHz (6th harmonic)	_____dBc	–60 dBc*
14.7 GHz (7th harmonic)	_____dBc	–60 dBc*
16.8 GHz (8th harmonic)	_____dBc	–60 dBc*
18.9 GHz (9th harmonic)	_____dBc	–60 dBc*
Set F1 to 3.6 GHz Record the level of all harmonics of the 3.6 GHz carrier:		
7.2 GHz (2nd harmonic)	_____dBc	–60 dBc*
10.8 GHz (3rd harmonic)	_____dBc	–60 dBc*
14.4 GHz (4th harmonic)	_____dBc	–60 dBc*
18.0 Ghz (5th harmonic)	_____dBc	–60 dBc*
Set F1 to 7.0 GHz Record the level of all harmonics of the 7 GHz carrier:		
14.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 10.0 GHz Record the level of all harmonics of the 10 GHz carrier:		
20.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc if Option 15A (High Power) installed.

3-9 Harmonic Test: RF Output Signals From 2 to 20 GHz (Continued)

Test Procedure (11 to 20 GHz)	Measure Value	Upper Limit
Set F1 to 12.4 GHz		
Record the level of all harmonics of the 12.4 GHz carrier:		
24.8 GHz (2nd harmonic)	_____dBc	–60 dBc*
37.2 GHz (3rd harmonic)	_____dBc	–60 dBc*
Set F1 to 16.0 GHz		
Record the level of all harmonics of the 16.0 GHz carrier:		
32.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 20.0 GHz		
Record the level of all harmonics of the 20.0 GHz carrier:		
40.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc if Option 15A (High Power) installed.

3-10 Single Sideband Phase Noise Test

Test Procedure	Measured Value	Upper Limit
Set F1 to 0.6 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–77 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc
Set F1 to 2.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–77 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc

3-10 Single Sideband Phase Noise Test (Continued)

Test Procedure	Measured Value	Upper Limit
Set F1 to 6.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–75 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 10.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–71 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 20.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–63 dBc
1 kHz	_____dBc	–92 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc
Set F1 to 26.5 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–60 dBc
1 kHz	_____dBc	–88 dBc
10 kHz	_____dBc	–91 dBc
100 kHz	_____dBc	–93 dBc

3-11 Power Level Accuracy and Flatness Tests (Model 69059A/69159A without Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz		Set F1 to 22.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+13 dBm	_____dBm	+ 9 dBm	_____dBm	+ 6 dBm	_____dBm
+12 dBm	_____dBm	+ 8 dBm	_____dBm	+ 5 dBm	_____dBm
+11 dBm	_____dBm	+ 7 dBm	_____dBm	+ 4 dBm	_____dBm
+10 dBm	_____dBm	+ 6 dBm	_____dBm	+ 3 dBm	_____dBm
+ 9 dBm	_____dBm	+ 5 dBm	_____dBm	+ 2 dBm	_____dBm
+ 8 dBm	_____dBm	+ 4 dBm	_____dBm	+ 1 dBm	_____dBm
+ 7 dBm	_____dBm	+ 3 dBm	_____dBm	+ 0 dBm	_____dBm
+ 6 dBm	_____dBm	+ 2 dBm	_____dBm	– 1 dBm	_____dBm
+ 5 dBm	_____dBm	+ 1 dBm	_____dBm	– 2 dBm	_____dBm
+ 4 dBm	_____dBm	+ 0 dBm	_____dBm	– 3 dBm	_____dBm
+ 3 dBm	_____dBm	– 1 dBm	_____dBm	– 4 dBm	_____dBm
+ 2 dBm	_____dBm	– 2 dBm	_____dBm	– 5 dBm	_____dBm
+ 1 dBm	_____dBm	– 3 dBm	_____dBm	– 6 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+ 6 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 1.6 dB (0.05 to 26.5 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69159A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+ 6 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 2.0 dB (0.05 to 20 GHz); 4.0 dB (20 to 26.5 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69059A/69159A with Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz		Set F1 to 22.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+11 dBm	_____dBm	+ 7 dBm	_____dBm	+ 3.5 dBm	_____dBm
+10 dBm	_____dBm	+ 6 dBm	_____dBm	+ 2.5 dBm	_____dBm
+ 9 dBm	_____dBm	+ 5 dBm	_____dBm	+ 1.5 dBm	_____dBm
+ 8 dBm	_____dBm	+ 4 dBm	_____dBm	+ 0.5 dBm	_____dBm
+ 7 dBm	_____dBm	+ 3 dBm	_____dBm	– 0.5 dBm	_____dBm
+ 6 dBm	_____dBm	+ 2 dBm	_____dBm	– 1.5 dBm	_____dBm
+ 5 dBm	_____dBm	+ 1 dBm	_____dBm	– 2.5 dBm	_____dBm
+ 4 dBm	_____dBm	+ 0 dBm	_____dBm	– 3.5 dBm	_____dBm
+ 3 dBm	_____dBm	– 1 dBm	_____dBm	– 4.5 dBm	_____dBm
+ 2 dBm	_____dBm	– 2 dBm	_____dBm	– 5.5 dBm	_____dBm
+ 1 dBm	_____dBm	– 3 dBm	_____dBm	– 6.5 dBm	_____dBm
+ 0 dBm	_____dBm	– 4 dBm	_____dBm	– 7.5 dBm	_____dBm
– 1 dBm	_____dBm	– 5 dBm	_____dBm	– 8.5 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+ 3.5 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 1.6 dB (0.05 to 26.5 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69159A only)

Set L1 to:	Max Power	Min Power	Variation ***
+ 3.5 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 7.0 dB (0.01 to 0.05 GHz); 6.0 dB (0.05 to 20 GHz); 8.2 dB (20 to 26.5 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69059A/69159A with Option 15A High Power & without Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz		Set F1 to 22.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+13 dBm	_____dBm	+13 dBm	_____dBm	+10 dBm	_____dBm
+12 dBm	_____dBm	+12 dBm	_____dBm	+ 9 dBm	_____dBm
+11 dBm	_____dBm	+11 dBm	_____dBm	+ 8 dBm	_____dBm
+10 dBm	_____dBm	+10 dBm	_____dBm	+ 7 dBm	_____dBm
+ 9 dBm	_____dBm	+ 9 dBm	_____dBm	+ 6 dBm	_____dBm
+ 8 dBm	_____dBm	+ 8 dBm	_____dBm	+ 5 dBm	_____dBm
+ 7 dBm	_____dBm	+ 7 dBm	_____dBm	+ 4 dBm	_____dBm
+ 6 dBm	_____dBm	+ 6 dBm	_____dBm	+ 3 dBm	_____dBm
+ 5 dBm	_____dBm	+ 5 dBm	_____dBm	+ 2 dBm	_____dBm
+ 4 dBm	_____dBm	+ 4 dBm	_____dBm	+ 1 dBm	_____dBm
+ 3 dBm	_____dBm	+ 3 dBm	_____dBm	+ 0 dBm	_____dBm
+ 2 dBm	_____dBm	+ 2 dBm	_____dBm	– 1 dBm	_____dBm
+ 1 dBm	_____dBm	+ 1 dBm	_____dBm	– 2 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+ 10 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 1.6 dB (0.05 to 26.5 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69159A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+ 10 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 2.0 dB (0.05 to 20 GHz); 4.0 dB (20 to 26.5 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69059A/69159A with Option 15A High Power & Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz		Set F1 to 22.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+11 dBm	_____dBm	+11 dBm	_____dBm	+ 7.5 dBm	_____dBm
+10 dBm	_____dBm	+10 dBm	_____dBm	+ 6.5 dBm	_____dBm
+ 9 dBm	_____dBm	+ 9 dBm	_____dBm	+ 5.5 dBm	_____dBm
+ 8 dBm	_____dBm	+ 8 dBm	_____dBm	+ 4.5 dBm	_____dBm
+ 7 dBm	_____dBm	+ 7 dBm	_____dBm	+ 3.5 dBm	_____dBm
+ 6 dBm	_____dBm	+ 6 dBm	_____dBm	+ 2.5 dBm	_____dBm
+ 5 dBm	_____dBm	+ 5 dBm	_____dBm	+ 1.5 dBm	_____dBm
+ 4 dBm	_____dBm	+ 4 dBm	_____dBm	+ 0.5 dBm	_____dBm
+ 3 dBm	_____dBm	+ 3 dBm	_____dBm	– 0.5 dBm	_____dBm
+ 2 dBm	_____dBm	+ 2 dBm	_____dBm	– 1.5 dBm	_____dBm
+ 1 dBm	_____dBm	+ 1 dBm	_____dBm	– 2.5 dBm	_____dBm
+ 0 dBm	_____dBm	+ 0 dBm	_____dBm	– 3.5 dBm	_____dBm
– 1 dBm	_____dBm	– 1 dBm	_____dBm	– 4.5 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+ 7.5 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 1.6 dB (0.05 to 26.5 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69159A only)

Set L1 to:	Max Power	Min Power	Variation ***
+ 7.5 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 7.0 dB (0.01 to 0.05 GHz); 6.0 dB (0.05 to 20 GHz); 8.2 dB (20 to 26.5 GHz)(typical, not a specification).

ANRITSU Model 69059A/69159A **Date:** _____

Serial Number _____ **Calibrated By:** _____

4-7 Preliminary Calibration

Procedure Step	**Step Completion**
1. Internal DVM Calibration (calterm119)	_____
2. Fine Loop Pretune DAC Calibration (calterm 136)	_____
3. Sweep Time DAC Calibration (calterm 132)	_____
4. YIG Frequency Offset DAC Calibration (calterm 134)	_____
5. YIG Frequency Linearizer DACs Calibration (calterm 127)	_____
6. 100 MHz Reference Oscillator Calibration (calterm 130)	_____
7. Ramp Center DAC Calibration (calterm 129)	_____
8. Sweep Width DAC Calibration (calterm 133)	_____
9. Center Frequency DAC Calibration (calterm 114)	_____
10. Store the Calibration Data	_____

4-8 Switched Filter Shaper Calibration

Log Amplifier Zero Calibration **Step Completion**

1. Log Amplifier Zero Calibration (calterm 115) . . . . . _____

Limiter DAC Adjustment (69059A/69159A's with Option 15A)

2. Limiter DAC Adjustment (calterm 145). . . . . _____

Shaper DAC Adjustment

2. Shaper DAC Adjustment (calterm 138) . . . . . _____
3. Store the Calibration Data . . . . . _____

4-9 RF Level Calibration

This calibration is performed using an automatic test system. Contact ANRITSU Customer Service for further information.

4-10 ALC Slope Calibration (69159A)

Procedure Step **Step Completion**

5. ALC Slope DAC adjustment . . . . . _____
6. Store the DAC setting value(s). . . . . _____

4-11 ALC Bandwidth Calibration

Procedure Step **Step Completion**

1. ALC Bandwidth Calibration (Calterm 110) . . . . . _____
2. Store the Calbration Data . . . . . _____

4-12 AM Calibration (69159A)

Procedure Step	Step Completion
2. Linear AM Calibration (calterm 112)	_____
3. Log AM Calibration (calterm 113)	_____
4. AM Meter Calibration (calterm 147)	_____
5. Store the Calibration Data	_____

4-13 FM Calibration (69159A)

Procedure Step	Step Completion
1. FM Meter Calibration (calterm 123)	_____
2. FM Variable Gain Linearity Calibration (calterm 148)	_____
3. FM Wide Calibration (calterm 124)	_____
4. FM Narrow Calibration (calterm 125)	_____
5. FM Rear Panel Input Gain Calibration (calterm 149)	_____
6. Store the Calibration Data	_____

ANRITSU Model 69063A/69163A **Date:** _____

Serial Number _____ **Tested By:** _____

3-6 Internal Time Base Aging Rate Test

Test Procedure	**Measured Value**	**Upper Limit**
Record frequency error value	_____	
Record frequency error value (after 24 hours)	_____	
Record the computed aging rate	_____per day	$2x10^{-8}$ per day ($5x10^{-10}$ per day with Option 16)

3-7 Frequency Synthesis Tests

Coarse Loop/YIG Loop Test Procedure

Test Frequency (in GHz)	Measured Value *	Test Frequency (in GHz)	Measured Value *
2.000 000 000	_____	21.000 000 000	_____
3.000 000 000	_____	22.000 000 000	_____
4.000 000 000	_____	23.000 000 000	_____
5.000 000 000	_____	24.000 000 000	_____
6.000 000 000	_____	25.000 000 000	_____
7.000 000 000	_____	26.000 000 000	_____
8.000 000 000	_____	27.000 000 000	_____
9.000 000 000	_____	28.000 000 000	_____
10.000 000 000	_____	29.000 000 000	_____
11.000 000 000	_____	30.000 000 000	_____
12.000 000 000	_____	31.000 000 000	_____
13.000 000 000	_____	32.000 000 000	_____
14.000 000 000	_____	33.000 000 000	_____
15.000 000 000	_____	34.000 000 000	_____
16.000 000 000	_____	35.000 000 000	_____
17.000 000 000	_____	36.000 000 000	_____
18.000 000 000	_____	37.000 000 000	_____
19.000 000 000	_____	38.000 000 000	_____
20.000 000 000	_____	39.000 000 000	_____
		40.000 000 000	_____

* Specification for all frequencies listed above is ±100 Hz.

3-7 Frequency Synthesis Tests (Continued)

Fine Loop Test Procedure (Standard 69X63A)

Test Frequency (in GHz)	Measured Value **
2.000 001 000	_____
2.000 002 000	_____
2.000 003 000	_____
2.000 004 000	_____
2.000 005 000	_____
2.000 006 000	_____
2.000 007 000	_____
2.000 008 000	_____
2.000 009 000	_____
2.000 010 000	_____

** Specification for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (69X63Awith Option 11)

Test Frequency (in GHz)	Measured Value ***
2.000 000 100	_____
2.000 000 200	_____
2.000 000 300	_____
2.000 000 400	_____
2.000 000 500	_____
2.000 000 600	_____
2.000 000 700	_____
2.000 000 800	_____
2.000 000 900	_____
2.000 001 000	_____

*** Specification for all frequencies listed above is ±10 Hz.

3-8 Spurious Signals Test: RF Output Signals <2 GHz

This test is not applicable to the 69063A/69163A model.

3-9 Harmonic Test: RF Output Signals From 2 to 20 GHz

Test Procedure (2 to 10 GHz)	**Measured Value**	**Upper Limit**
Set F1 to 2.1 GHz		
Record the level of all harmonics of the 2.1 GHz carrier:		
4.2 GHz (2nd harmonic)	_____dBc	–60 dBc*
6.3 GHz (3rd harmonic)	_____dBc	–60 dBc*
8.4 GHz (4th harmonic)	_____dBc	–60 dBc*
10.5 GHz (5th harmonic)	_____dBc	–60 dBc*
12.6 GHz (6th harmonic)	_____dBc	–60 dBc*
14.7 GHz (7th harmonic)	_____dBc	–60 dBc*
16.8 GHz (8th harmonic)	_____dBc	–60 dBc*
18.9 GHz (9th harmonic)	_____dBc	–60 dBc*
Set F1 to 3.6 GHz		
Record the level of all harmonics of the 3.6 GHz carrier:		
7.2 GHz (2nd harmonic)	_____dBc	–60 dBc*
10.8 GHz (3rd harmonic)	_____dBc	–60 dBc*
14.4 GHz (4th harmonic)	_____dBc	–60 dBc*
18.0 Ghz (5th harmonic)	_____dBc	–60 dBc*
Set F1 to 7.0 GHz		
Record the level of all harmonics of the 7 GHz carrier:		
14.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 10.0 GHz		
Record the level of all harmonics of the 10 GHz carrier:		
20.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc if Option 15A (High Power) installed.

3-9 Harmonic Test: RF Output Signals From 2 to 20 GHz (Continued)

Test Procedure (11 to 20 GHz)	**Measured Value**	**Upper Limit**
Set F1 to 12.4 GHz Record the level of all harmonics of the 12.4 GHz carrier:		
24.8 GHz (2nd harmonic)	_____dBc	–60 dBc*
37.2 GHz (3rd harmonic)	_____dBc	–60 dBc*
Set F1 to 16.0 GHz Record the level of all harmonics of the 16.0 GHz carrier:		
32.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 20.0 GHz Record the level of all harmonics of the 20.0 GHz carrier:		
40.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc if Option 15A (High Power) installed.

3-10 Single Sideband Phase Noise Test

Test Procedure	Measured Value	Upper Limit
Set F1 to 2.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–77 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 6.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–75 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 10.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–71 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 20.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–63 dBc
1 kHz	_____dBc	–92 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc
Set F1 to 26.5 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–60 dBc
1 kHz	_____dBc	–88 dBc
10 kHz	_____dBc	–91 dBc
100 kHz	_____dBc	–93 dBc

3-11 Power Level Accuracy and Flatness Tests (Model 69063A/69163A without Option 2B Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz		Set F1 to 25.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+ 9 dBm	_____dBm	+ 6 dBm	_____dBm
+ 8 dBm	_____dBm	+ 5 dBm	_____dBm
+ 7 dBm	_____dBm	+ 4 dBm	_____dBm
+ 6 dBm	_____dBm	+ 3 dBm	_____dBm
+ 5 dBm	_____dBm	+ 2dBm	_____dBm
+ 4 dBm	_____dBm	+ 1 dBm	_____dBm
+ 3 dBm	_____dBm	+ 0 dBm	_____dBm
+ 2 dBm	_____dBm	– 1 dBm	_____dBm
+ 1 dBm	_____dBm	– 2 dBm	_____dBm
+ 0 dBm	_____dBm	– 3 dBm	_____dBm
– 1 dBm	_____dBm	– 4 dBm	_____dBm
– 2 dBm	_____dBm	– 5 dBm	_____dBm
– 3 dBm	_____dBm	– 6 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+ 6 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69163A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+ 6 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (2 to 20 GHz); 4.0 dB (20 to 40 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69063A/69163A with Option 2B Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz		Set F1 to 25.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+ 7 dBm	_____dBm	+ 3 dBm	_____dBm
+ 6 dBm	_____dBm	+ 2 dBm	_____dBm
+ 5 dBm	_____dBm	+ 1 dBm	_____dBm
+ 4 dBm	_____dBm	+ 0 dBm	_____dBm
+ 3 dBm	_____dBm	– 1 dBm	_____dBm
+ 2 dBm	_____dBm	– 2 dBm	_____dBm
+ 1 dBm	_____dBm	– 3 dBm	_____dBm
+ 0 dBm	_____dBm	– 4 dBm	_____dBm
– 1 dBm	_____dBm	– 5 dBm	_____dBm
– 2 dBm	_____dBm	– 6 dBm	_____dBm
– 3 dBm	_____dBm	– 7 dBm	_____dBm
– 4 dBm	_____dBm	– 8 dBm	_____dBm
– 5 dBm	_____dBm	– 9 dBm	_____dBm

* Specification is ±1.0 dB.

* Specification is ±1.0 dB.

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+ 3 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69163A only)

Set L1 to:	Max Power	Min Power	Variation ***
+ 3 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 6.0 dB (2 to 20 GHz); 8.2 dB (20 to 40 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69063A/69163A with Option 15A High Power & without Option 2B Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz		Set F1 to 25.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+13 dBm	_____dBm	+ 6 dBm	_____dBm
+12 dBm	_____dBm	+ 5 dBm	_____dBm
+11 dBm	_____dBm	+ 4 dBm	_____dBm
+10 dBm	_____dBm	+ 3 dBm	_____dBm
+ 9 dBm	_____dBm	+ 2 dBm	_____dBm
+ 8 dBm	_____dBm	+ 1 dBm	_____dBm
+ 7 dBm	_____dBm	+ 0 dBm	_____dBm
+ 6 dBm	_____dBm	– 1 dBm	_____dBm
+ 5 dBm	_____dBm	– 2 dBm	_____dBm
+ 4 dBm	_____dBm	– 3 dBm	_____dBm
+ 3 dBm	_____dBm	– 4 dBm	_____dBm
+ 2 dBm	_____dBm	– 5 dBm	_____dBm
+ 1 dBm	_____dBm	– 6 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+ 6 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69163A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+ 6 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (2 to 20 GHz); 4.0 dB (20 to 40 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69063A/69163A with Option 15A High Power & Option 2B Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz		Set F1 to 25.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+11 dBm	_____dBm	+ 3 dBm	_____dBm
+10 dBm	_____dBm	+ 2 dBm	_____dBm
+ 9 dBm	_____dBm	+ 1 dBm	_____dBm
+ 8 dBm	_____dBm	+ 0 dBm	_____dBm
+ 7 dBm	_____dBm	– 1 dBm	_____dBm
+ 6 dBm	_____dBm	– 2 dBm	_____dBm
+ 5 dBm	_____dBm	– 3 dBm	_____dBm
+ 4 dBm	_____dBm	– 4 dBm	_____dBm
+ 3 dBm	_____dBm	– 5 dBm	_____dBm
+ 2 dBm	_____dBm	– 6 dBm	_____dBm
+ 1 dBm	_____dBm	– 7 dBm	_____dBm
+ 0 dBm	_____dBm	– 8 dBm	_____dBm
– 1 dBm	_____dBm	– 9 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+ 3 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69163A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+ 3 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 6.0 dB (2 to 20 GHz); 8.2 dB (20 to 40 GHz)(typical, not a specification).

ANRITSU Model 69063A/69163A **Date:** _____

Serial Number _____ **Calibrated By:** _____

4-7 Preliminary Calibration

Procedure Step	**Step Completion**
1. Internal DVM Calibration (calterm119)	_____
2. Fine Loop Pretune DAC Calibration (calterm 136)	_____
3. Sweep Time DAC Calibration (calterm 132)	_____
4. YIG Frequency Offset DAC Calibration (calterm 134)	_____
5. YIG Frequency Linearizer DACs Calibration (calterm 127)	_____
6. 100 MHz Reference Oscillator Calibration (calterm 130)	_____
7. Ramp Center DAC Calibration (calterm 129)	_____
8. Sweep Width DAC Calibration (calterm 133)	_____
9. Center Frequency DAC Calibration (calterm 114)	_____
10. Store the Calibration Data	_____

4-8 Switched Filter Shaper Calibration

Log Amplifier Zero Calibration **Step Completion**

1. Log Amplifier Zero Calibration (calterm 115) . . . . . _____

Limiter DAC Adjustment (69063A/69163A with Option 15A)

2. Limiter DAC Adjustment (calterm 145). . . . . _____

Shaper DAC Adjustment

2. Shaper DAC Adjustment (calterm 138) . . . . . _____
3. Store the Calibration Data . . . . . _____

4-9 RF Level Calibration

This calibration is performed using an automatic test system. Contact ANRITSU Customer Service for further information.

4-10 ALC Slope Calibration (69163A)

Procedure Step **Step Completion**

5. ALC Slope DAC adjustment . . . . . _____
6. Store the DAC setting value(s). . . . . _____

4-11 ALC Bandwidth Calibration

Procedure Step **Step Completion**

1. ALC Bandwidth Calibration (Calterm 110) . . . . . _____
2. Store the DAC setting values . . . . . _____

4-12 AM Calibration (69163A)

Procedure Step	Step Completion
2. Linear AM Calibration (calterm 112)	_____
3. Log AM Calibration (calterm 113)	_____
4. AM Meter Calibration (calterm 147)	_____
5. Store the Calibration Data	_____

4-13 FM Calibration (69163A)

Procedure Step	Step Completion
1. FM Meter Calibration (calterm 123)	_____
2. FM Variable Gain Linearity Calibration (calterm 148)	_____
3. FM Wide Sensitivity Calibration (calterm 124)	_____
4. FM Narrow Sensitivity Calibration (calterm 125)	_____
5. FM Rear Panel Input Gain Calibration (calterm 149)	_____
6. Store the Calibration Data	_____

ANRITSU Model 69065A/69165A **Date:** _____

Serial Number _____ **Tested By:** _____

3-6 Internal Time Base Aging Rate Test

Test Procedure	**Measured Value**	**Upper Limit**
Record frequency error value	_____	
Record frequency error value (after 24 hours)	_____	
Record the computed aging rate	_____per day	$2x10^{-8}$ per day ($5x10^{-10}$ per day with Option 16)

3-7 Frequency Synthesis Tests

Coarse Loop/YIG Loop Test Procedure

Test Frequency (in GHz)	Measured Value *	Test Frequency (in GHz)	Measured Value *
1.000 000 000	_____	21.000 000 000	_____
2.000 000 000	_____	22.000 000 000	_____
3.000 000 000	_____	23.000 000 000	_____
4.000 000 000	_____	24.000 000 000	_____
5.000 000 000	_____	25.000 000 000	_____
6.000 000 000	_____	26.000 000 000	_____
7.000 000 000	_____	27.000 000 000	_____
8.000 000 000	_____	28.000 000 000	_____
9.000 000 000	_____	29.000 000 000	_____
10.000 000 000	_____	30.000 000 000	_____
11.000 000 000	_____	31.000 000 000	_____
12.000 000 000	_____	32.000 000 000	_____
13.000 000 000	_____	33.000 000 000	_____
14.000 000 000	_____	34.000 000 000	_____
15.000 000 000	_____	35.000 000 000	_____
16.000 000 000	_____	36.000 000 000	_____
17.000 000 000	_____	37.000 000 000	_____
18.000 000 000	_____	38.000 000 000	_____
19.000 000 000	_____	39.000 000 000	_____
20.000 000 000	_____	40.000 000 000	_____

* Specification for all frequencies listed above is ±100 Hz.

3-7 Frequency Synthesis Tests (Continued)

Fine Loop Test Procedure (Standard 69X65A)

Test Frequency (in Ghz)	Measured Value **
1.000 001 000	_____
1.000 002 000	_____
1.000 003 000	_____
1.000 004 000	_____
1.000 005 000	_____
1.000 006 000	_____
1.000 007 000	_____
1.000 008 000	_____
1.000 009 000	_____
1.000 010 000	_____

** Specifications for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (69X65A with Option 11)

Test Frequency (in Ghz)	Measured Value ***
1.000 000 100	_____
1.000 000 200	_____
1.000 000 300	_____
1.000 000 400	_____
1.000 000 500	_____
1.000 000 600	_____
1.000 000 700	_____
1.000 000 800	_____
1.000 000 900	_____
1.000 001 000	_____

*** Specification for all frequencies listed above is ±10 Hz.

3-8 Spurious Signals Test: RF Output Signals <2.2 GHz

Test Procedure	Measured Value	Upper Limit
Set F1 to 500 MHz Record the level of all harmonics of the 500 MHz carrier		
1.0 GHz (2nd harmonic)	_____dBc	–50 dBc
1.5 GHz (3rd harmonic)	_____dBc	–50 dBc
2.0 GHz (4th harmonic)	_____dBc	–50 dBc
2.5 GHz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 800 MHz Record the level of all harmonics of the 800 MHz carrier		
1.6 GHz (2nd harmonic)	_____dBc	–50 dBc
2.4 GHz (3rd harmonic)	_____dBc	–50 dBc
3.2 GHz (4th harmonic)	_____dBc	–50 dBc
4.0 GHz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 1.3 GHz Record the level of all harmonics of the 1.3 GHz carrier		
2.6 GHz (2nd harmonic)	_____dBc	–50 dBc
3.9 GHz (3rd harmonic)	_____dBc	–50 dBc
5.2 GHz (4th harmonic)	_____dBc	–50 dBc
6.5 GHz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 2.1 GHz Record the level of all harmonics of the 2.1 GHz carrier		
4.2 GHz (2nd harmonic)	_____dBc	–50 dBc
6.3 GHz (3rd harmonic)	_____dBc	–50 dBc
8.2 GHz (4th harmonic)	_____dBc	–50 dBc
10.2 GHz (5th harmonic)	_____dBc	–50 dBc

3-9 Harmonic Test: RF Output Signals From 2.2 to 20 GHz

Test Procedure (2.2 to 10 GHz)	Measure Value	Upper Limit
Set F1 to 2.4 GHz		
Record the level of all harmonics of the 2.4 GHz carrier:		
4.8 GHz (2nd harmonic)	_____dBc	–60 dBc*
7.2 GHz (3rd harmonic)	_____dBc	–60 dBc*
9.6 GHz (4th harmonic)	_____dBc	–60 dBc*
12.0 GHz (5th harmonic)	_____dBc	–60 dBc*
14.4 GHz (6th harmonic)	_____dBc	–60 dBc*
16.8 GHz (7th harmonic)	_____dBc	–60 dBc*
19.2 GHz (8th harmonic)	_____dBc	–60 dBc*
Set F1 to 3.6 GHz		
Record the level of all harmonics of the 3.6 GHz carrier:		
7.2 GHz (2nd harmonic)	_____dBc	–60 dBc*
10.8 GHz (3rd harmonic)	_____dBc	–60 dBc*
14.4 GHz (4th harmonic)	_____dBc	–60 dBc*
18.0 Ghz (5th harmonic)	_____dBc	–60 dBc*
Set F1 to 7.0 GHz		
Record the level of all harmonics of the 7 GHz carrier:		
14.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 10.0 GHz		
Record the level of all harmonics of the 10 GHz carrier:		
20.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc in Option 15A (High Power) installed.

3-9 Harmonic Test: RF Output Signals From 2.2 to 20 GHz (Continued)

Test Procedure (11 to 20 GHz)	Measure Value	Upper Limit
Set F1 to 12.4 GHz		
Record the level of all harmonics of the 12.4 GHz carrier:		
24.8 GHz (2nd harmonic)	_____dBc	–60 dBc*
37.2 GHz (3rd harmonic)	_____dBc	–60 dBc*
Set F1 to 16.0 GHz		
Record the level of all harmonics of the 16.0 GHz carrier:		
32.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 20.0 GHz		
Record the level of all harmonics of the 20.0 GHz carrier:		
40.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc if Option 15A (High Power) installed.

3-10 Single Sideband Phase Noise Test

Test Procedure	Measured Value	Upper Limit
Set F1 to 0.6 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–89 dBc
1 kHz	_____dBc	–109 dBc
10 kHz	_____dBc	–109 dBc
100 kHz	_____dBc	–114 dBc
Set F1 to 2.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–83 dBc
1 kHz	_____dBc	–103 dBc
10 kHz	_____dBc	–103 dBc
100 kHz	_____dBc	–108 dBc

3-10 Single Sideband Phase Noise Test (Continued)

Test Procedure	Measured Value	Upper Limit
Set F1 to 6.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–75 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 10.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–71 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 20.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–63 dBc
1 kHz	_____dBc	–92 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc
Set F1 to 26.5 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–60 dBc
1 kHz	_____dBc	–88 dBc
10 kHz	_____dBc	–91 dBc
100 kHz	_____dBc	–93 dBc

3-11 Power Level Accuracy and Flatness Tests (Model 69065A/69165A without Option 2B Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz		Set F1 to 25.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+13 dBm	_____dBm	+ 9 dBm	_____dBm	+ 6dBm	_____dBm
+12 dBm	_____dBm	+ 8 dBm	_____dBm	+ 5 dBm	_____dBm
+11 dBm	_____dBm	+ 7 dBm	_____dBm	+ 4 dBm	_____dBm
+10 dBm	_____dBm	+ 6 dBm	_____dBm	+ 3 dBm	_____dBm
+ 9 dBm	_____dBm	+ 5 dBm	_____dBm	+ 2dBm	_____dBm
+ 8 dBm	_____dBm	+ 4 dBm	_____dBm	+ 1 dBm	_____dBm
+ 7 dBm	_____dBm	+ 3 dBm	_____dBm	+ 0 dBm	_____dBm
+ 6 dBm	_____dBm	+ 2 dBm	_____dBm	– 1 dBm	_____dBm
+ 5 dBm	_____dBm	+ 1 dBm	_____dBm	– 2 dBm	_____dBm
+ 4 dBm	_____dBm	+ 0 dBm	_____dBm	– 3 dBm	_____dBm
+ 3 dBm	_____dBm	– 1 dBm	_____dBm	– 4 dBm	_____dBm
+ 2 dBm	_____dBm	– 2 dBm	_____dBm	– 5 dBm	_____dBm
+ 1 dBm	_____dBm	– 3 dBm	_____dBm	– 6 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+ 6 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69165A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+ 6 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (0.5 to 20 GHz); 4.0 dB (20 to 40 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69065A/69165A with Option 2B Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz		Set F1 to 25.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+11 dBm	_____dBm	+ 7 dBm	_____dBm	+ 3 dBm	_____dBm
+10 dBm	_____dBm	+ 6 dBm	_____dBm	+ 2 dBm	_____dBm
+ 9 dBm	_____dBm	+ 5 dBm	_____dBm	+ 1 dBm	_____dBm
+ 8 dBm	_____dBm	+ 4 dBm	_____dBm	+ 0 dBm	_____dBm
+ 7 dBm	_____dBm	+ 3 dBm	_____dBm	– 1 dBm	_____dBm
+ 6 dBm	_____dBm	+ 2 dBm	_____dBm	– 2 dBm	_____dBm
+ 5 dBm	_____dBm	+ 1 dBm	_____dBm	– 3 dBm	_____dBm
+ 4 dBm	_____dBm	+ 0 dBm	_____dBm	– 4 dBm	_____dBm
+ 3 dBm	_____dBm	– 1 dBm	_____dBm	– 5 dBm	_____dBm
+ 2 dBm	_____dBm	– 2 dBm	_____dBm	– 6 dBm	_____dBm
+ 1 dBm	_____dBm	– 3 dBm	_____dBm	– 7 dBm	_____dBm
+ 0 dBm	_____dBm	– 4 dBm	_____dBm	– 8 dBm	_____dBm
– 1 dBm	_____dBm	– 5 dBm	_____dBm	– 9 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+ 3 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69165A only)

Set L1 to:	Max Power	Min Power	Variation ***
+ 3 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 6.0 dB (0.5 to 20 GHz); 8.2 dB (20 to 40 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69065A/69165A with Option 15A High Power & without Option 2B Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz		Set F1 to 25.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+13 dBm	_____dBm	+13 dBm	_____dBm	+ 6 dBm	_____dBm
+12 dBm	_____dBm	+12 dBm	_____dBm	+ 5 dBm	_____dBm
+11 dBm	_____dBm	+11 dBm	_____dBm	+ 4 dBm	_____dBm
+10 dBm	_____dBm	+10 dBm	_____dBm	+ 3 dBm	_____dBm
+ 9 dBm	_____dBm	+ 9 dBm	_____dBm	+ 2 dBm	_____dBm
+ 8 dBm	_____dBm	+ 8 dBm	_____dBm	+ 1 dBm	_____dBm
+ 7 dBm	_____dBm	+ 7 dBm	_____dBm	+ 0 dBm	_____dBm
+ 6 dBm	_____dBm	+ 6 dBm	_____dBm	– 1 dBm	_____dBm
+ 5 dBm	_____dBm	+ 5 dBm	_____dBm	– 2 dBm	_____dBm
+ 4 dBm	_____dBm	+ 4 dBm	_____dBm	– 3 dBm	_____dBm
+ 3 dBm	_____dBm	+ 3 dBm	_____dBm	– 4 dBm	_____dBm
+ 2 dBm	_____dBm	+ 2 dBm	_____dBm	– 5 dBm	_____dBm
+ 1 dBm	_____dBm	+ 1 dBm	_____dBm	– 6 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+ 6 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69165A only)

Set L1 to:	Max Power	Min Power	Variation ***
+ 6 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (0.5 to 20 GHz); 4.0 dB (20 to 40 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69065A/69165A with Option 15A High Power & Option 2B Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz		Set F1 to 25.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+11 dBm	_____dBm	+11 dBm	_____dBm	+ 3 dBm	_____dBm
+10 dBm	_____dBm	+10 dBm	_____dBm	+ 2 dBm	_____dBm
+ 9 dBm	_____dBm	+ 9 dBm	_____dBm	+ 1 dBm	_____dBm
+ 8 dBm	_____dBm	+ 8 dBm	_____dBm	+ 0 dBm	_____dBm
+ 7 dBm	_____dBm	+ 7 dBm	_____dBm	– 1 dBm	_____dBm
+ 6 dBm	_____dBm	+ 6 dBm	_____dBm	– 2 dBm	_____dBm
+ 5 dBm	_____dBm	+ 5 dBm	_____dBm	– 3 dBm	_____dBm
+ 4 dBm	_____dBm	+ 4 dBm	_____dBm	– 4 dBm	_____dBm
+ 3 dBm	_____dBm	+ 3 dBm	_____dBm	– 5 dBm	_____dBm
+ 2 dBm	_____dBm	+ 2 dBm	_____dBm	– 6 dBm	_____dBm
+ 1 dBm	_____dBm	+ 1 dBm	_____dBm	– 7 dBm	_____dBm
+ 0 dBm	_____dBm	+ 0 dBm	_____dBm	– 8 dBm	_____dBm
– 1 dBm	_____dBm	– 1 dBm	_____dBm	– 9 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+ 3 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep) (Model 69165A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+ 3 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 6.0 dB (0.5 to 20 GHz); 8.2 dB (20 to 40 GHz)(typical, not a specification).

ANRITSU Model 69065A/69165A **Date:** _____

Serial Number _____ **Calibrated By:** _____

4-7 Preliminary Calibration

Procedure Step	**Step Completion**
1. Internal DVM Calibration (calterm119)	_____
2. Fine Loop Pretune DAC Calibration (calterm 136)	_____
3. Sweep Time DAC Calibration (calterm 132)	_____
4. YIG Frequency Offset DAC Calibration (calterm 134)	_____
5. YIG Frequency Linearizer DACs Calibration (calterm 127)	_____
6. 100 MHz Reference Oscillator Calibration (calterm 130)	_____
7. Ramp Center DAC Calibration (calterm 129)	_____
8. Sweep Width DAC Calibration (calterm 133)	_____
9. Center Frequency DAC Calibration (calterm 114)	_____
10. Store the Calibration Data	_____

4-8 Switched Filter Shaper Calibration

Log Amplifier Zero Calibration **Step Completion**

1. Log Amplifier Zero Calibration (calterm 115) . . . . . _____

Limiter DAC Adjustment (69065A/69165A's with Option 15A)

2. Limiter DAC Adjustment (calterm 145). . . . . _____

Shaper DAC Adjustment

2. Shaper DAC Adjustment (calterm 138) . . . . . _____
3. Store the Calibration Data . . . . . _____

4-9 RF Level Calibration

This calibration is performed using an automatic test system. Contact ANRITSU Customer Service for further information.

4-10 ALC Slope Calibration (69165A)

Procedure Step **Step Completion**

5. ALC Slope DAC adjustment . . . . . _____
6. Store the DAC setting value(s). . . . . _____

4-11 ALC Bandwidth Calibration

Procedure Step **Step Completion**

1. ALC Bandwidth Calibration (Calterm 110) . . . . . _____
2. Store the Calibration Data . . . . . _____

4-12 AM Calibration (69165A)

Procedure Step	Step Completion
2. Linear AM Calibration (calterm 112)	_____
3. Log AM Calibration (calterm 113)	_____
4. AM Meter Calibration (calterm 147)	_____
5. Store the Calibration Data	_____

4-13 FM Calibration (69165A)

Procedure Step	Step Completion
1. FM Meter Calibration (calterm 123)	_____
2. FM Variable Gain Linearity Calibration (calterm 148)	_____
3. FM Wide Sensitivity Calibration (calterm 124)	_____
4. FM Narrow Sensitivity Calibration (calterm 125)	_____
5. FM Rear Panel Input Gain Calibration (calterm 149)	_____
6. Store the Calibration Data	_____

ANRITSU Model 69069A/69169A **Date:** _____

Serial Number _____ **Tested By:** _____

3-6 Internal Time Base Aging Rate Test

Test Procedure	Measured Value	Upper Limit
Record frequency error value	_____	
Record frequency error value (after 24 hours)	_____	
Record the computed aging rate	_____per day	$2x10^{-8}$ per day ($5x10^{-10}$ per day with Option 16)

3-7 Frequency Synthesis Tests

Coarse Loop/YIG Loop Test Procedure

Test Frequency (in GHz)	Measured Value *	Test Frequency (in GHz)	Measured Value *
1.000 000 000	_____	21.000 000 000	_____
2.000 000 000	_____	22.000 000 000	_____
3.000 000 000	_____	23.000 000 000	_____
4.000 000 000	_____	24.000 000 000	_____
5.000 000 000	_____	25.000 000 000	_____
6.000 000 000	_____	26.000 000 000	_____
7.000 000 000	_____	27.000 000 000	_____
8.000 000 000	_____	28.000 000 000	_____
9.000 000 000	_____	29.000 000 000	_____
10.000 000 000	_____	30.000 000 000	_____
11.000 000 000	_____	31.000 000 000	_____
12.000 000 000	_____	32.000 000 000	_____
13.000 000 000	_____	33.000 000 000	_____
14.000 000 000	_____	34.000 000 000	_____
15.000 000 000	_____	35.000 000 000	_____
16.000 000 000	_____	36.000 000 000	_____
17.000 000 000	_____	37.000 000 000	_____
18.000 000 000	_____	38.000 000 000	_____
19.000 000 000	_____	39.000 000 000	_____
20.000 000 000	_____	40.000 000 000	_____

* Specification for all frequencies listed above is ±100 Hz.

3-7 Frequency Synthesis Tests (Continued)

Fine Loop Test Procedure (Standard 69X69A)

Test Frequency (in Ghz)	Measured Value **
1.000 001 000	_____
1.000 002 000	_____
1.000 003 000	_____
1.000 004 000	_____
1.000 005 000	_____
1.000 006 000	_____
1.000 007 000	_____
1.000 008 000	_____
1.000 009 000	_____
1.000 010 000	_____

** Specifications for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (69X69A with Option 11)

Test Frequency (in Ghz)	Measured Value ***
1.000 000 100	_____
1.000 000 200	_____
1.000 000 300	_____
1.000 000 400	_____
1.000 000 500	_____
1.000 000 600	_____
1.000 000 700	_____
1.000 000 800	_____
1.000 000 900	_____
1.000 001 000	_____

*** Specification for all frequencies listed above is ±10 Hz.

3-8 Spurious Signals Test: RF Output Signals <2 GHz

Test Procedure	Measured Value	Upper Limit
Set F1 to 10 MHz		
Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 20 MHz		
Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 30 MHz		
Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 40 MHz		
Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 350 MHz		
Record the presence of the worst case harmonic	_____dBc	–40 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 1.6 GHz		
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 1.6 GHz		
Record the level of the harmonics of the 1.6 GHz carrier:		
3.2 GHz (2nd harmonic)	_____dBc	–40 dBc
4.8 GHz (3rd harmonic)	_____dBc	–40 dBc

3-9 Harmonic Test: RF Output Signals From 2 to 20 GHz

Test Procedure (2 to 10 GHz)	**Measure Value**	**Upper Limit**
Set F1 to 2.1 GHz Record the level of all harmonics of the 2.1 GHz carrier:		
4.2 GHz (2nd harmonic)	_____dBc	–60 dBc*
6.3 GHz (3rd harmonic)	_____dBc	–60 dBc*
8.4 GHz (4th harmonic)	_____dBc	–60 dBc*
10.5 GHz (5th harmonic)	_____dBc	–60 dBc*
12.6 GHz (6th harmonic)	_____dBc	–60 dBc*
14.7 GHz (7th harmonic)	_____dBc	–60 dBc*
16.8 GHz (8th harmonic)	_____dBc	–60 dBc*
18.9 GHz (9th harmonic)	_____dBc	–60 dBc*
Set F1 to 3.6 GHz Record the level of all harmonics of the 3.6 GHz carrier:		
7.2 GHz (2nd harmonic)	_____dBc	–60 dBc*
10.8 GHz (3rd harmonic)	_____dBc	–60 dBc*
14.4 GHz (4th harmonic)	_____dBc	–60 dBc*
18.0 Ghz (5th harmonic)	_____dBc	–60 dBc*
Set F1 to 7.0 GHz Record the level of all harmonics of the 7 GHz carrier:		
14.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 10.0 GHz Record the level of all harmonics of the 10 GHz carrier:		
20.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc in Option 15A (High Power) installed.

3-9 Harmonic Test: RF Output Signals From 2 to 20 GHz (Continued)

Test Procedure (11 to 20 GHz)	Measure Value	Upper Limit
Set F1 to 12.4 GHz		
Record the level of all harmonics of the 12.4 GHz carrier:		
24.8 GHz (2nd harmonic)	_____dBc	–60 dBc*
37.2 GHz (3rd harmonic)	_____dBc	–60 dBc*
Set F1 to 16.0 GHz		
Record the level of all harmonics of the 16.0 GHz carrier:		
32.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 20.0 GHz		
Record the level of all harmonics of the 20.0 GHz carrier:		
40.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc if Option 15A (High Power) installed.

3-10 Single Sideband Phase Noise Test

Test Procedure	Measured Value	Upper Limit
Set F1 to 0.6 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–77 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc
Set F1 to 2.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–77 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc

3-10 Single Sideband Phase Noise Test (Continued)

Test Procedure	Measured Value	Upper Limit
Set F1 to 6.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–75 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 10.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–71 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 20.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–63 dBc
1 kHz	_____dBc	–92 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc
Set F1 to 26.5 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–60 dBc
1 kHz	_____dBc	–88 dBc
10 kHz	_____dBc	–91 dBc
100 kHz	_____dBc	–93 dBc

3-11 Power Level Accuracy and Flatness Tests (Model 69069A/69169A without Option 2B Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz		Set F1 to 25.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+13 dBm	_____dBm	+ 9 dBm	_____dBm	+ 6dBm	_____dBm
+12 dBm	_____dBm	+ 8 dBm	_____dBm	+ 5 dBm	_____dBm
+11 dBm	_____dBm	+ 7 dBm	_____dBm	+ 4 dBm	_____dBm
+10 dBm	_____dBm	+ 6 dBm	_____dBm	+ 3 dBm	_____dBm
+ 9 dBm	_____dBm	+ 5 dBm	_____dBm	+ 2dBm	_____dBm
+ 8 dBm	_____dBm	+ 4 dBm	_____dBm	+ 1 dBm	_____dBm
+ 7 dBm	_____dBm	+ 3 dBm	_____dBm	+ 0 dBm	_____dBm
+ 6 dBm	_____dBm	+ 2 dBm	_____dBm	– 1 dBm	_____dBm
+ 5 dBm	_____dBm	+ 1 dBm	_____dBm	– 2 dBm	_____dBm
+ 4 dBm	_____dBm	+ 0 dBm	_____dBm	– 3 dBm	_____dBm
+ 3 dBm	_____dBm	– 1 dBm	_____dBm	– 4 dBm	_____dBm
+ 2 dBm	_____dBm	– 2 dBm	_____dBm	– 5 dBm	_____dBm
+ 1 dBm	_____dBm	– 3 dBm	_____dBm	– 6 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+ 6 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 1.6 dB (0.05 to 40 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69169A only)

Set L1 to:	Max Power	Min Power	Variation ***
+ 6 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 2.0 dB (0.05 to 20 GHz); 4.0 dB (20 to 40 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69069A/69169A with Option 2B Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz		Set F1 to 25.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+11 dBm	_____dBm	+ 7 dBm	_____dBm	+ 3 dBm	_____dBm
+10 dBm	_____dBm	+ 6 dBm	_____dBm	+ 2 dBm	_____dBm
+ 9 dBm	_____dBm	+ 5 dBm	_____dBm	+ 1 dBm	_____dBm
+ 8 dBm	_____dBm	+ 4 dBm	_____dBm	+ 0 dBm	_____dBm
+ 7 dBm	_____dBm	+ 3 dBm	_____dBm	– 1 dBm	_____dBm
+ 6 dBm	_____dBm	+ 2 dBm	_____dBm	– 2 dBm	_____dBm
+ 5 dBm	_____dBm	+ 1 dBm	_____dBm	– 3 dBm	_____dBm
+ 4 dBm	_____dBm	+ 0 dBm	_____dBm	– 4 dBm	_____dBm
+ 3 dBm	_____dBm	– 1 dBm	_____dBm	– 5 dBm	_____dBm
+ 2 dBm	_____dBm	– 2 dBm	_____dBm	– 6 dBm	_____dBm
+ 1 dBm	_____dBm	– 3 dBm	_____dBm	– 7 dBm	_____dBm
+ 0 dBm	_____dBm	– 4 dBm	_____dBm	– 8 dBm	_____dBm
– 1 dBm	_____dBm	– 5 dBm	_____dBm	– 9 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+ 3 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 1.6 dB (0.05 to 40 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69169A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+ 3 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 7.0 dB (0.01 to 0.05 GHz); 6.0 dB (0.05 to 20 GHz); 8.2 dB (20 to 40 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69069A/69169A with Option 15A High Power & without Option 2B Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz		Set F1 to 25.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+13 dBm	_____dBm	+13 dBm	_____dBm	+ 6 dBm	_____dBm
+12 dBm	_____dBm	+12 dBm	_____dBm	+ 5 dBm	_____dBm
+11 dBm	_____dBm	+11 dBm	_____dBm	+ 4 dBm	_____dBm
+10 dBm	_____dBm	+10 dBm	_____dBm	+ 3 dBm	_____dBm
+ 9 dBm	_____dBm	+ 9 dBm	_____dBm	+ 2 dBm	_____dBm
+ 8 dBm	_____dBm	+ 8 dBm	_____dBm	+ 1 dBm	_____dBm
+ 7 dBm	_____dBm	+ 7 dBm	_____dBm	+ 0 dBm	_____dBm
+ 6 dBm	_____dBm	+ 6 dBm	_____dBm	– 1 dBm	_____dBm
+ 5 dBm	_____dBm	+ 5 dBm	_____dBm	– 2 dBm	_____dBm
+ 4 dBm	_____dBm	+ 4 dBm	_____dBm	– 3 dBm	_____dBm
+ 3 dBm	_____dBm	+ 3 dBm	_____dBm	– 4 dBm	_____dBm
+ 2 dBm	_____dBm	+ 2 dBm	_____dBm	– 5 dBm	_____dBm
+ 1 dBm	_____dBm	+ 1 dBm	_____dBm	– 6 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+ 6 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 1.6 dB (0.05 to 40 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69169A only)

Set L1 to:	Max Power	Min Power	Variation ***
+ 6 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 2.0 dB (0.05 to 20 GHz); 4.0 dB (20 to 40 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69069A/69169A with Option 15A High Power & Option 2B Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz		Set F1 to 25.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+11 dBm	_____dBm	+11 dBm	_____dBm	+ 3 dBm	_____dBm
+10 dBm	_____dBm	+10 dBm	_____dBm	+ 2 dBm	_____dBm
+ 9 dBm	_____dBm	+ 9 dBm	_____dBm	+ 1 dBm	_____dBm
+ 8 dBm	_____dBm	+ 8 dBm	_____dBm	+ 0 dBm	_____dBm
+ 7 dBm	_____dBm	+ 7 dBm	_____dBm	– 1 dBm	_____dBm
+ 6 dBm	_____dBm	+ 6 dBm	_____dBm	– 2 dBm	_____dBm
+ 5 dBm	_____dBm	+ 5 dBm	_____dBm	– 3 dBm	_____dBm
+ 4 dBm	_____dBm	+ 4 dBm	_____dBm	– 4 dBm	_____dBm
+ 3 dBm	_____dBm	+ 3 dBm	_____dBm	– 5 dBm	_____dBm
+ 2 dBm	_____dBm	+ 2 dBm	_____dBm	– 6 dBm	_____dBm
+ 1 dBm	_____dBm	+ 1 dBm	_____dBm	– 7 dBm	_____dBm
+ 0 dBm	_____dBm	+ 0 dBm	_____dBm	– 8 dBm	_____dBm
– 1 dBm	_____dBm	– 1 dBm	_____dBm	– 9 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.0 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+ 3 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 1.6 dB (0.05 to 40 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69169A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+ 3 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 7.0 dB (0.01 to 0.05 GHz); 6.0 dB (0.05 to 20 GHz); 8.2 dB (20 to 40 GHz)(typical, not a specification).

ANRITSU Model 69069A/69169A **Date:** _____

Serial Number _____ **Calibrated By:** _____

4-7 Preliminary Calibration

Procedure Step	**Step Completion**
1. Internal DVM Calibration (calterm119)	_____
2. Fine Loop Pretune DAC Calibration (calterm 136)	_____
3. Sweep Time DAC Calibration (calterm 132)	_____
4. YIG Frequency Offset DAC Calibration (calterm 134)	_____
5. YIG Frequency Linearizer DACs Calibration (calterm 127)	_____
6. 100 MHz Reference Oscillator Calibration (calterm 130)	_____
7. Ramp Center DAC Calibration (calterm 129)	_____
8. Sweep Width DAC Calibration (calterm 133)	_____
9. Center Frequency DAC Calibration (calterm 114)	_____
10. Store the Calibration Data	_____

4-8 Switched Filter Shaper Calibration

Log Amplifier Zero Calibration **Step Completion**

1. Log Amplifier Zero Calibration (calterm 115) . . . . . _____

Limiter DAC Adjustment (69069A/69169A's with Option 15A)

2. Limiter DAC Adjustment (calterm 145). . . . . _____

Shaper DAC Adjustment

2. Shaper DAC Adjustment (calterm 138) . . . . . _____
3. Store the Calibration Data . . . . . _____

4-9 RF Level Calibration

This calibration is performed using an automatic test system. Contact ANRITSU Customer Service for further information.

4-10 ALC Slope Calibration (69169A)

Procedure Step **Step Completion**

5. ALC Slope DAC adjustment . . . . . _____
6. Store the DAC setting value(s). . . . . _____

4-11 ALC Bandwidth Calibration

Procedure Step **Step Completion**

1. ALC Bandwidth Calibration (Calterm 110) . . . . . _____
2. Store the Calibration Data . . . . . _____

4-12 AM Calibration (69169A)

Procedure Step	Step Completion
2. Linear AM Calibration (calterm 112)	_____
3. Log AM Calibration (calterm 113)	_____
4. AM Meter Calibration (calterm 147)	_____
5. Store the Calibration Data	_____

4-13 FM Calibration (69169A)

Procedure Step	Step Completion
1. FM Meter Calibration (calterm 123)	_____
2. FM Variable Gain Linearity Calibration (calterm 148)	_____
3. FM Wide Sensitivity Calibration (calterm 124)	_____
4. FM Narrow Sensitivity Calibration (calterm 125)	_____
5. FM Rear Panel Input Gain Calibration (calterm 149)	_____
6. Store the Calibration Data	_____

ANRITSU Model 69075A/69175A **Date:** _____

Serial Number _____ **Tested By:** _____

3-6 Internal Time Base Aging Rate Test

Test Procedure	Measured Value	Upper Limit
Record frequency error value	_____	
Record frequency error value (after 24 hours)	_____	
Record the computed aging rate	_____per day	$2x10^{-8}$ per day ($5x10^{-10}$ per day with Option 16)

3-7 Frequency Synthesis Tests

Coarse Loop/YIG Loop Test Procedure

Test Frequency (in GHz)	Measured Value *	Test Frequency (in GHz)	Measured Value *
1.000 000 000	_____	26.000 000 000	_____
2.000 000 000	_____	27.000 000 000	_____
3.000 000 000	_____	28.000 000 000	_____
4.000 000 000	_____	29.000 000 000	_____
5.000 000 000	_____	30.000 000 000	_____
6.000 000 000	_____	31.000 000 000	_____
7.000 000 000	_____	32.000 000 000	_____
8.000 000 000	_____	33.000 000 000	_____
9.000 000 000	_____	34.000 000 000	_____
10.000 000 000	_____	35.000 000 000	_____
11.000 000 000	_____	36.000 000 000	_____
12.000 000 000	_____	37.000 000 000	_____
13.000 000 000	_____	38.000 000 000	_____
14.000 000 000	_____	39.000 000 000	_____
15.000 000 000	_____	40.000 000 000	_____
16.000 000 000	_____	41.000 000 000	_____
17.000 000 000	_____	42.000 000 000	_____
18.000 000 000	_____	43.000 000 000	_____
19.000 000 000	_____	44.000 000 000	_____
20.000 000 000	_____	45.000 000 000	_____
21.000 000 000	_____	46.000 000 000	_____
22.000 000 000	_____	47.000 000 000	_____
23.000 000 000	_____	48.000 000 000	_____
24.000 000 000	_____	49.000 000 000	_____
25.000 000 000	_____	50.000 000 000	_____

* Specification for all frequencies listed above is ±100 Hz.

3-7 Frequency Synthesis Tests (Continued)

Fine Loop Test Procedure (Standard 69X75A)

Test Frequency (in Ghz)	Measured Value **
1.000 001 000	_____
1.000 002 000	_____
1.000 003 000	_____
1.000 004 000	_____
1.000 005 000	_____
1.000 006 000	_____
1.000 007 000	_____
1.000 008 000	_____
1.000 009 000	_____
1.000 010 000	_____

** Specifications for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (69X75A with Option 11)

Test Frequency (in Ghz)	Measured Value ***
1.000 000 100	_____
1.000 000 200	_____
1.000 000 300	_____
1.000 000 400	_____
1.000 000 500	_____
1.000 000 600	_____
1.000 000 700	_____
1.000 000 800	_____
1.000 000 900	_____
1.000 001 000	_____

*** Specification for all frequencies listed above is ±10 Hz.

3-8 Spurious Signals Test: RF Output Signals <2.2 GHz

Test Procedure	Measured Value	Upper Limit
Set F1 to 500 MHz Record the level of all harmonics of the 500 MHz carrier		
1.0 GHz (2nd harmonic)	_____dBc	–50 dBc
1.5 GHz (3rd harmonic)	_____dBc	–50 dBc
2.0 GHz (4th harmonic)	_____dBc	–50 dBc
2.5 GHz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 800 MHz Record the level of all harmonics of the 800 MHz carrier		
1.6 GHz (2nd harmonic)	_____dBc	–50 dBc
2.4 GHz (3rd harmonic)	_____dBc	–50 dBc
3.2 GHz (4th harmonic)	_____dBc	–50 dBc
4.0 GHz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 1.3 GHz Record the level of all harmonics of the 1.3 GHz carrier		
2.6 GHz (2nd harmonic)	_____dBc	–50 dBc
3.9 GHz (3rd harmonic)	_____dBc	–50 dBc
5.2 GHz (4th harmonic)	_____dBc	–50 dBc
6.5 GHz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 2.1 GHz Record the level of all harmonics of the 2.1 GHz carrier		
4.2 GHz (2nd harmonic)	_____dBc	–50 dBc
6.3 GHz (3rd harmonic)	_____dBc	–50 dBc
8.2 GHz (4th harmonic)	_____dBc	–50 dBc
10.2 GHz (5th harmonic)	_____dBc	–50 dBc

3-9 Harmonic Test: RF Output Signals From 2.2 to 20 GHz

Test Procedure (2.2 to 10 GHz)	**Measure Value**	**Upper Limit**
Set F1 to 2.4 GHz Record the level of all harmonics of the 2.4 GHz carrier:		
4.8 GHz (2nd harmonic)	_____dBc	–50 dBc
7.2 GHz (3rd harmonic)	_____dBc	–50 dBc
9.6 GHz (4th harmonic)	_____dBc	–50 dBc
12.0 GHz (5th harmonic)	_____dBc	–50 dBc
14.4 GHz (6th harmonic)	_____dBc	–50 dBc
16.8 GHz (7th harmonic)	_____dBc	–50 dBc
19.2 GHz (8th harmonic)	_____dBc	–50 dBc
Set F1 to 3.6 GHz Record the level of all harmonics of the 3.6 GHz carrier:		
7.2 GHz (2nd harmonic)	_____dBc	–50 dBc
10.8 GHz (3rd harmonic)	_____dBc	–50 dBc
14.4 GHz (4th harmonic)	_____dBc	–50 dBc
18.0 Ghz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 7.0 GHz Record the level of all harmonics of the 7 GHz carrier:		
14.0 GHz (2nd harmonic)	_____dBc	–50 dBc
Set F1 to 10.0 GHz Record the level of all harmonics of the 10 GHz carrier:		
20.0 GHz (2nd harmonic)	_____dBc	–50 dBc

Test Procedure (11 to 20 GHz)		
Set F1 to 12.4 GHz Record the level of all harmonics of the 12.4 GHz carrier:		
24.8 GHz (2nd harmonic)	_____dBc	–50 dBc
37.2 GHz (3rd harmonic)	_____dBc	–50 dBc
Set F1 to 16.0 GHz Record the level of all harmonics of the 16.0 GHz carrier:		
32.0 GHz (2nd harmonic)	_____dBc	–50 dBc
Set F1 to 20.0 GHz Record the level of all harmonics of the 20.0 GHz carrier:		
40.0 GHz (2nd harmonic)	_____dBc	–50 dBc

3-10 Single Sideband Phase Noise Test

Test Procedure	Measured Value	Upper Limit
Set F1 to 0.6 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–89 dBc
1 kHz	_____dBc	–109 dBc
10 kHz	_____dBc	–109 dBc
100 kHz	_____dBc	–114 dBc
Set F1 to 2.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–83 dBc
1 kHz	_____dBc	–103 dBc
10 kHz	_____dBc	–103 dBc
100 kHz	_____dBc	–108 dBc
Set F1 to 6.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–75 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 10.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–71 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 20.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–63 dBc
1 kHz	_____dBc	–92 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc

3-10 Single Sideband Phase Noise Test (Continued)

Test Procedure	Measured Value	Upper Limit
Set F1 to 26.5 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–60 dBc
1 kHz	_____dBc	–88 dBc
10 kHz	_____dBc	–91 dBc
100 kHz	_____dBc	–93 dBc

3-11 Power Level Accuracy and Flatness Tests (Model 69075A/69175A without Option 2C Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz		Set F1 to 25.0 GHz		Set F1 to 45.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+10 dBm	_____dBm	+ 2.5 dBm	_____dBm	+ 2.5 dBm	_____dBm
+ 9 dBm	_____dBm	+ 1.5 dBm	_____dBm	+ 1.5 dBm	_____dBm
+ 8 dBm	_____dBm	+ 0.5 dBm	_____dBm	+ 0.5 dBm	_____dBm
+ 7 dBm	_____dBm	– 0.5 dBm	_____dBm	– 0.5 dBm	_____dBm
+ 6 dBm	_____dBm	– 1.5 dBm	_____dBm	– 1.5 dBm	_____dBm
+ 5 dBm	_____dBm	– 2.5 dBm	_____dBm	– 2.5 dBm	_____dBm
+ 4 dBm	_____dBm	– 3.5 dBm	_____dBm	– 3.5 dBm	_____dBm
+ 3 dBm	_____dBm	– 4.5 dBm	_____dBm	– 4.5 dBm	_____dBm
+ 2 dBm	_____dBm	– 5.5 dBm	_____dBm	– 5.5 dBm	_____dBm
+ 1 dBm	_____dBm	– 6.5 dBm	_____dBm	– 6.5 dBm	_____dBm
0 dBm	_____dBm	– 7.5 dBm	_____dBm	– 7.5 dBm	_____dBm
– 1 dBm	_____dBm	– 8.5 dBm	_____dBm	– 8.5 dBm	_____dBm
– 2 dBm	_____dBm	– 9.5 dBm	_____dBm	– 9.5 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.5 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+ 2.5 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB (0.5 to 40 GHz); 2.2 dB (40 to 50 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69175A only)

Set L1 to:	Max Power	Min Power	Variation ***
+ 2.5 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (0.5 to 20 GHz); 4.0 dB (20 to 40 GHz); 5.0 dB (40 to 50 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69075A/69175A with Option 2C Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz		Set F1 to 25.0 GHz		Set F1 to 45.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+ 8.5 dBm	_____dBm	+ 0 dBm	_____dBm	– 1 dBm	_____dBm
+ 7.5 dBm	_____dBm	– 1 dBm	_____dBm	– 2 dBm	_____dBm
+ 6.5 dBm	_____dBm	– 2 dBm	_____dBm	– 3 dBm	_____dBm
+ 5.5 dBm	_____dBm	– 3 dBm	_____dBm	– 4 dBm	_____dBm
+ 4.5 dBm	_____dBm	– 4 dBm	_____dBm	– 5 dBm	_____dBm
+ 3.5 dBm	_____dBm	– 5 dBm	_____dBm	– 6 dBm	_____dBm
+ 2.5 dBm	_____dBm	– 6 dBm	_____dBm	– 7 dBm	_____dBm
+ 1.5 dBm	_____dBm	– 7 dBm	_____dBm	– 8 dBm	_____dBm
+ 0.5 dBm	_____dBm	– 8 dBm	_____dBm	– 9 dBm	_____dBm
– 0.5 dBm	_____dBm	– 9 dBm	_____dBm	–10 dBm	_____dBm
– 1.5 dBm	_____dBm	–10 dBm	_____dBm	–11 dBm	_____dBm
– 2.5 dBm	_____dBm	– 11 dBm	_____dBm	–12 dBm	_____dBm
– 3.5 dBm	_____dBm	– 12 dBm	_____dBm	–13 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.5 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
– 1 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB (0.05 to 40 GHz); 2.2 dB (40 to 50 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69175A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
– 1 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 6.0 dB (0.05 to 20 GHz); 8.2 dB (20 to 40 GHz); 10.2 dB (40 to 50 GHz)(typical, not a specification).

ANRITSU Model 69075A/69175A **Date:** _____

Serial Number _____ **Calibrated By:** _____

4-7 Preliminary Calibration

Procedure Step	**Step Completion**
1. Internal DVM Calibration (calterm119)	_____
2. Fine Loop Pretune DAC Calibration (calterm 136)	_____
3. Sweep Time DAC Calibration (calterm 132)	_____
4. YIG Frequency Offset DAC Calibration (calterm 134)	_____
5. YIG Frequency Linearizer DACs Calibration (calterm 127)	_____
6. 100 MHz Reference Oscillator Calibration (calterm 130)	_____
7. Ramp Center DAC Calibration (calterm 129)	_____
8. Sweep Width DAC Calibration (calterm 133)	_____
9. Center Frequency DAC Calibration (calterm 114)	_____
10. Store the Calibration Data	_____

4-8 Switched Filter Shaper Calibration

Log Amplifier Zero Calibration **Step Completion**

1. Log Amplifier Zero Calibration (calterm 115) . . . . . _____

Limiter DAC Adjustment

2. Limiter DAC Adjustment (calterm 145). . . . . _____

Shaper DAC Adjustment

2. Shaper DAC Adjustment (calterm 138) . . . . . _____
3. Store the Calibration Data . . . . . _____

4-9 RF Level Calibration

This calibration is performed using an automatic test system. Contact ANRITSU Customer Service for further information.

4-10 ALC Slope Calibration (69175A)

Procedure Step **Step Completion**

3. ALC Slope DAC adjustment . . . . . _____
4. Store the DAC setting value(s). . . . . _____

4-11 ALC Bandwidth Calibration

Procedure Step **Step Completion**

1. ALC Bandwidth Calibration (Calterm 110) . . . . . _____
2. Store the Calibration Data . . . . . _____

4-12 AM Calibration (69175A)

Procedure Step	Step Completion
2. Linear AM Calibration (calterm 112)	_____
3. Log AM Calibration (calterm 113)	_____
4. AM Meter Calibration (calterm 147)	_____
5. Store the Calibration Data	_____

4-13 FM Calibration (69175A)

Procedure Step	Step Completion
1. FM Meter Calibration (calterm 123)	_____
2. FM Variable Gain Linearity Calibration (calterm 148)	_____
3. FM Wide Sensitivity Calibration (calterm 124)	_____
4. FM Narrow Sensitivity Calibration (calterm 125)	_____
5. FM Rear Panel Input Gain Calibration (calterm 149)	_____
6. Store the Calibration Data	_____

ANRITSU Model 69077A/69177A **Date:** _____

Serial Number _____ **Tested By:** _____

3-6 Internal Time Base Aging Rate Test

Test Procedure	Measured Value	Upper Limit
Record frequency error value	_____	
Record frequency error value (after 24 hours)	_____	
Record the computed aging rate	_____per day	$2x10^{-8}$ per day ($5x10^{-10}$ per day with Option 16)

3-7 Frequency Synthesis Tests

Coarse Loop/YIG Loop Test Procedure

Test Frequency (in GHz)	Measured Value *	Test Frequency (in GHz)	Measured Value *
1.000 000 000	_____	26.000 000 000	_____
2.000 000 000	_____	27.000 000 000	_____
3.000 000 000	_____	28.000 000 000	_____
4.000 000 000	_____	29.000 000 000	_____
5.000 000 000	_____	30.000 000 000	_____
6.000 000 000	_____	31.000 000 000	_____
7.000 000 000	_____	32.000 000 000	_____
8.000 000 000	_____	33.000 000 000	_____
9.000 000 000	_____	34.000 000 000	_____
10.000 000 000	_____	35.000 000 000	_____
11.000 000 000	_____	36.000 000 000	_____
12.000 000 000	_____	37.000 000 000	_____
13.000 000 000	_____	38.000 000 000	_____
14.000 000 000	_____	39.000 000 000	_____
15.000 000 000	_____	40.000 000 000	_____
16.000 000 000	_____	41.000 000 000	_____
17.000 000 000	_____	42.000 000 000	_____
18.000 000 000	_____	43.000 000 000	_____
19.000 000 000	_____	44.000 000 000	_____
20.000 000 000	_____	45.000 000 000	_____
21.000 000 000	_____	46.000 000 000	_____
22.000 000 000	_____	47.000 000 000	_____
23.000 000 000	_____	48.000 000 000	_____
24.000 000 000	_____	49.000 000 000	_____
25.000 000 000	_____	50.000 000 000	_____

* Specification for all frequencies listed above is ±100 Hz.

3-7 Frequency Synthesis Tests (Continued)

Fine Loop Test Procedure (Standard 69X77A)

Test Frequency (in Ghz)	Measured Value **
1.000 001 000	_____
1.000 002 000	_____
1.000 003 000	_____
1.000 004 000	_____
1.000 005 000	_____
1.000 006 000	_____
1.000 007 000	_____
1.000 008 000	_____
1.000 009 000	_____
1.000 010 000	_____

** Specifications for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (69X77A with Option 11)

Test Frequency (in Ghz)	Measured Value ***
1.000 000 100	_____
1.000 000 200	_____
1.000 000 300	_____
1.000 000 400	_____
1.000 000 500	_____
1.000 000 600	_____
1.000 000 700	_____
1.000 000 800	_____
1.000 000 900	_____
1.000 001 000	_____

*** Specification for all frequencies listed above is ±10 Hz.

3-8 Spurious Signals Test: RF Output Signals <2 GHz

Test Procedure	Measured Value	Upper Limit
Set F1 to 10 MHz		
Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 20 MHz		
Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 30 MHz		
Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 40 MHz		
Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 350 MHz		
Record the presence of the worst case harmonic	_____dBc	–40 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 1.6 GHz		
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 1.6 GHz		
Record the level of the harmonics of the 1.6 GHz carrier:		
3.2 GHz (2nd harmonic)	_____dBc	–40 dBc
4.8 GHz (3rd harmonic)	_____dBc	–40 dBc

3-9 Harmonic Test: RF Output Signals From 2 to 20 GHz

Test Procedure (2 to 10 GHz)	**Measure Value**	**Upper Limit**
Set F1 to 2.1 GHz Record the level of all harmonics of the 2.1 GHz carrier:		
4.2 GHz (2nd harmonic)	_____dBc	–50 dBc
6.3 GHz (3rd harmonic)	_____dBc	–50 dBc
8.4 GHz (4th harmonic)	_____dBc	–50 dBc
10.5 GHz (5th harmonic)	_____dBc	–50 dBc
12.6 GHz (6th harmonic)	_____dBc	–50 dBc
14.7 GHz (7th harmonic)	_____dBc	–50 dBc
16.8 GHz (8th harmonic)	_____dBc	–50 dBc
18.9 GHz (9th harmonic)	_____dBc	–50 dBc
Set F1 to 3.6 GHz Record the level of all harmonics of the 3.6 GHz carrier:		
7.2 GHz (2nd harmonic)	_____dBc	–50 dBc
10.8 GHz (3rd harmonic)	_____dBc	–50 dBc
14.4 GHz (4th harmonic)	_____dBc	–50 dBc
18.0 Ghz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 7.0 GHz Record the level of all harmonics of the 7 GHz carrier:		
14.0 GHz (2nd harmonic)	_____dBc	–50 dBc
Set F1 to 10.0 GHz Record the level of all harmonics of the 10 GHz carrier:		
20.0 GHz (2nd harmonic)	_____dBc	–50 dBc

Test Procedure (11 to 20 GHz)		
Set F1 to 12.4 GHz Record the level of all harmonics of the 12.4 GHz carrier:		
24.8 GHz (2nd harmonic)	_____dBc	–50 dBc
37.2 GHz (3rd harmonic)	_____dBc	–50 dBc
Set F1 to 16.0 GHz Record the level of all harmonics of the 16.0 GHz carrier:		
32.0 GHz (2nd harmonic)	_____dBc	–50 dBc
Set F1 to 20.0 GHz Record the level of all harmonics of the 20.0 GHz carrier:		
40.0 GHz (2nd harmonic)	_____dBc	–50 dBc

3-10 Single Sideband Phase Noise Test

Test Procedure	Measured Value	Upper Limit
Set F1 to 0.6 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–74 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc
Set F1 to 2.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–77 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 6.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–75 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 10.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–71 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 20.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–63 dBc
1 kHz	_____dBc	–92 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc

3-10 Single Sideband Phase Noise Test (Continued)

Test Procedure	Measured Value	Upper Limit
Set F1 to 26.5 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–60 dBc
1 kHz	_____dBc	–88 dBc
10 kHz	_____dBc	–91 dBc
100 kHz	_____dBc	–93 dBc

3-11 Power Level Accuracy and Flatness Tests (Model 69077A/69177A without Option 2C Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz		Set F1 to 25.0 GHz		Set F1 to 45.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+10 dBm	_____dBm	+ 2.5 dBm	_____dBm	+ 2.5 dBm	_____dBm
+ 9 dBm	_____dBm	+ 1.5 dBm	_____dBm	+ 1.5 dBm	_____dBm
+ 8 dBm	_____dBm	+ 0.5 dBm	_____dBm	+ 0.5 dBm	_____dBm
+ 7 dBm	_____dBm	– 0.5 dBm	_____dBm	– 0.5 dBm	_____dBm
+ 6 dBm	_____dBm	– 1.5 dBm	_____dBm	– 1.5 dBm	_____dBm
+ 5 dBm	_____dBm	– 2.5 dBm	_____dBm	– 2.5 dBm	_____dBm
+ 4 dBm	_____dBm	– 3.5 dBm	_____dBm	– 3.5 dBm	_____dBm
+ 3 dBm	_____dBm	– 4.5 dBm	_____dBm	– 4.5 dBm	_____dBm
+ 2 dBm	_____dBm	– 5.5 dBm	_____dBm	– 5.5 dBm	_____dBm
+ 1 dBm	_____dBm	– 6.5 dBm	_____dBm	– 6.5 dBm	_____dBm
0 dBm	_____dBm	– 7.5 dBm	_____dBm	– 7.5 dBm	_____dBm
– 1 dBm	_____dBm	– 8.5 dBm	_____dBm	– 8.5 dBm	_____dBm
– 2 dBm	_____dBm	– 9.5 dBm	_____dBm	– 9.5 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.5 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+ 2.5 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 1.6 dB (0.05 to 40 GHz); 2.2 dB (40 to 50 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69177A only)

Set L1 to:	Max Power	Min Power	Variation ***
+ 2.5 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 2.0 dB (0.05 to 20 GHz); 4.0 dB (20 to 40 GHz); 5.0 dB (40 to 50 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69077A/69177A with Option 2C Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz		Set F1 to 25.0 GHz		Set F1 to 45.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+ 8.5 dBm	_____dBm	+ 0 dBm	_____dBm	– 1 dBm	_____dBm
+ 7.5 dBm	_____dBm	– 1 dBm	_____dBm	– 2 dBm	_____dBm
+ 6.5 dBm	_____dBm	– 2 dBm	_____dBm	– 3 dBm	_____dBm
+ 5.5 dBm	_____dBm	– 3 dBm	_____dBm	– 4 dBm	_____dBm
+ 4.5 dBm	_____dBm	– 4 dBm	_____dBm	– 5 dBm	_____dBm
+ 3.5 dBm	_____dBm	– 5 dBm	_____dBm	– 6 dBm	_____dBm
+ 2.5 dBm	_____dBm	– 6 dBm	_____dBm	– 7 dBm	_____dBm
+ 1.5 dBm	_____dBm	– 7 dBm	_____dBm	– 8 dBm	_____dBm
+ 0.5 dBm	_____dBm	– 8 dBm	_____dBm	– 9 dBm	_____dBm
– 0.5 dBm	_____dBm	– 9 dBm	_____dBm	–10 dBm	_____dBm
– 1.5 dBm	_____dBm	–10 dBm	_____dBm	–11 dBm	_____dBm
– 2.5 dBm	_____dBm	– 11 dBm	_____dBm	–12 dBm	_____dBm
– 3.5 dBm	_____dBm	– 12 dBm	_____dBm	–13 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.5 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
– 1 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 1.6 dB (0.05 to 40 GHz); 2.2 dB (40 to 50 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69177A only)

Set L1 to:	Max Power	Min Power	Variation ***
– 1 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 7.0 dB (0.01 to 0.05 GHz); 6.0 dB (0.05 to 20 GHz); 8.2 dB (20 to 40 GHz); 10.2 dB (40 to 50 GHz)(typical, not a specification).

ANRITSU Model 69077A/69177A **Date:** _____

Serial Number _____ **Calibrated By:** _____

4-7 Preliminary Calibration

Procedure Step	**Step Completion**
1. Internal DVM Calibration (calterm119)	_____
2. Fine Loop Pretune DAC Calibration (calterm 136)	_____
3. Sweep Time DAC Calibration (calterm 132)	_____
4. YIG Frequency Offset DAC Calibration (calterm 134)	_____
5. YIG Frequency Linearizer DACs Calibration (calterm 127)	_____
6. 100 MHz Reference Oscillator Calibration (calterm 130)	_____
7. Ramp Center DAC Calibration (calterm 129)	_____
8. Sweep Width DAC Calibration (calterm 133)	_____
9. Center Frequency DAC Calibration (calterm 114)	_____
10. Store the Calibration Data	_____

4-8 Switched Filter Shaper Calibration

Log Amplifier Zero Calibration **Step Completion**

1. Log Amplifier Zero Calibration (calterm 115) . . . . . _____

Limiter DAC Adjustment

2. Limiter DAC Adjustment (calterm 145). . . . . _____

Shaper DAC Adjustment

2. Shaper DAC Adjustment (calterm 138) . . . . . _____
3. Store the Calibration Data . . . . . _____

4-9 RF Level Calibration

This calibration is performed using an automatic test system. Contact ANRITSU Customer Service for further information.

4-10 ALC Slope Calibration (69177A)

Procedure Step **Step Completion**

3. ALC Slope DAC adjustment . . . . . _____
4. Store the DAC setting value(s). . . . . _____

4-11 ALC Bandwidth Calibration

Procedure Step **Step Completion**

1. ALC Bandwidth Calibration (Calterm 110) . . . . . _____
2. Store the Calibration Data . . . . . _____

4-12 AM Calibration (69177A)

Procedure Step	Step Completion
2. Linear AM Calibration (calterm 112)	_____
3. Log AM Calibration (calterm 113)	_____
4. AM Meter Calibration (calterm 147)	_____
5. Store the Calibration Data	_____

4-13 FM Calibration (69177A)

Procedure Step	Step Completion
1. FM Meter Calibration (calterm 123)	_____
2. FM Variable Gain Linearity Calibration (calterm 148)	_____
3. FM Wide Sensitivity Calibration (calterm 124)	_____
4. FM Narrow Sensitivity Calibration (calterm 125)	_____
5. FM Rear Panel Input Gain Calibration (calterm 149)	_____
6. Store the Calibration Data	_____

ANRITSU Model 69085A/69185A **Date:** _____

Serial Number _____ **Tested By:** _____

3-6 Internal Time Base Aging Rate Test

Test Procedure	**Measured Value**	**Upper Limit**
Record frequency error value	_____	
Record frequency error value (after 24 hours)	_____	
Record the computed aging rate	_____per day	$2x10^{-8}$ per day ($5x10^{-10}$ per day with Option 16)

3-7 Frequency Synthesis Tests

Coarse Loop/YIG Loop Test Procedure

Test Frequency (in GHz)	Measured Value *	Test Frequency (in GHz)	Measured Value *
1.000 000 000	_____	26.000 000 000	_____
2.000 000 000	_____	27.000 000 000	_____
3.000 000 000	_____	28.000 000 000	_____
4.000 000 000	_____	29.000 000 000	_____
5.000 000 000	_____	30.000 000 000	_____
6.000 000 000	_____	31.000 000 000	_____
7.000 000 000	_____	32.000 000 000	_____
8.000 000 000	_____	33.000 000 000	_____
9.000 000 000	_____	34.000 000 000	_____
10.000 000 000	_____	35.000 000 000	_____
11.000 000 000	_____	36.000 000 000	_____
12.000 000 000	_____	37.000 000 000	_____
13.000 000 000	_____	38.000 000 000	_____
14.000 000 000	_____	39.000 000 000	_____
15.000 000 000	_____	40.000 000 000	_____
16.000 000 000	_____	41.000 000 000	_____
17.000 000 000	_____	42.000 000 000	_____
18.000 000 000	_____	43.000 000 000	_____
19.000 000 000	_____	44.000 000 000	_____
20.000 000 000	_____	45.000 000 000	_____
21.000 000 000	_____	46.000 000 000	_____
22.000 000 000	_____	47.000 000 000	_____
23.000 000 000	_____	48.000 000 000	_____
24.000 000 000	_____	49.000 000 000	_____
25.000 000 000	_____	50.000 000 000	_____

3-7 Frequency Synthesis Tests (Continued)

Coarse Loop/YIG Loop Test Procedure (Continued)

Test Frequency (in GHz)	Measured Value *	Test Frequency (in GHz)	Measured Value *
51.000 000 000	_____	56.000 000 000	_____
52.000 000 000	_____	57.000 000 000	_____
53.000 000 000	_____	58.000 000 000	_____
54.000 000 000	_____	59.000 000 000	_____
55.000 000 000	_____	60.000 000 000	_____

* Specification for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (Standard 69X85A)

Test Frequency (in Ghz)	Measured Value **
1.000 001 000	_____
1.000 002 000	_____
1.000 003 000	_____
1.000 004 000	_____
1.000 005 000	_____
1.000 006 000	_____
1.000 007 000	_____
1.000 008 000	_____
1.000 009 000	_____
1.000 010 000	_____
	_____

** Specifications for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (69X85A with Option 11)

Test Frequency (in Ghz)	Measured Value ***
1.000 000 100	_____
1.000 000 200	_____
1.000 000 300	_____
1.000 000 400	_____
1.000 000 500	_____
1.000 000 600	_____
1.000 000 700	_____
1.000 000 800	_____
1.000 000 900	_____
1.000 001 000	_____

*** Specification for all frequencies listed above is ±10 Hz.

3-8 Spurious Signals Test: RF Output Signals <2.2 GHz

Test Procedure	Measured Value	Upper Limit
Set F1 to 500 MHz Record the level of all harmonics of the 500 MHz carrier		
1.0 GHz (2nd harmonic)	_____dBc	–50 dBc
1.5 GHz (3rd harmonic)	_____dBc	–50 dBc
2.0 GHz (4th harmonic)	_____dBc	–50 dBc
2.5 GHz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 800 MHz Record the level of all harmonics of the 800 MHz carrier		
1.6 GHz (2nd harmonic)	_____dBc	–50 dBc
2.4 GHz (3rd harmonic)	_____dBc	–50 dBc
3.2 GHz (4th harmonic)	_____dBc	–50 dBc
4.0 GHz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 1.3 GHz Record the level of all harmonics of the 1.3 GHz carrier		
2.6 GHz (2nd harmonic)	_____dBc	–50 dBc
3.9 GHz (3rd harmonic)	_____dBc	–50 dBc
5.2 GHz (4th harmonic)	_____dBc	–50 dBc
6.5 GHz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 2.1 GHz Record the level of all harmonics of the 2.1 GHz carrier		
4.2 GHz (2nd harmonic)	_____dBc	–50 dBc
6.3 GHz (3rd harmonic)	_____dBc	–50 dBc
8.2 GHz (4th harmonic)	_____dBc	–50 dBc
10.2 GHz (5th harmonic)	_____dBc	–50 dBc

3-9 Harmonic Test: RF Output Signals From 2.2 to 20 GHz

Test Procedure (2.2 to 10 GHz)	**Measure Value**	**Upper Limit**
Set F1 to 2.4 GHz Record the level of all harmonics of the 2.4 GHz carrier:		
4.8 GHz (2nd harmonic)	_____dBc	–50 dBc
7.2 GHz (3rd harmonic)	_____dBc	–50 dBc
9.6 GHz (4th harmonic)	_____dBc	–50 dBc
12.0 GHz (5th harmonic)	_____dBc	–50 dBc
14.4 GHz (6th harmonic)	_____dBc	–50 dBc
16.8 GHz (7th harmonic)	_____dBc	–50 dBc
19.2 GHz (8th harmonic)	_____dBc	–50 dBc
Set F1 to 3.6 GHz Record the level of all harmonics of the 3.6 GHz carrier:		
7.2 GHz (2nd harmonic)	_____dBc	–50 dBc
10.8 GHz (3rd harmonic)	_____dBc	–50 dBc
14.4 GHz (4th harmonic)	_____dBc	–50 dBc
18.0 Ghz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 7.0 GHz Record the level of all harmonics of the 7 GHz carrier:		
14.0 GHz (2nd harmonic)	_____dBc	–50 dBc
Set F1 to 10.0 GHz Record the level of all harmonics of the 10 GHz carrier:		
20.0 GHz (2nd harmonic)	_____dBc	–50 dBc

Test Procedure (11 to 20 GHz)		
Set F1 to 12.4 GHz Record the level of all harmonics of the 12.4 GHz carrier:		
24.8 GHz (2nd harmonic)	_____dBc	–50 dBc
37.2 GHz (3rd harmonic)	_____dBc	–50 dBc
Set F1 to 16.0 GHz Record the level of all harmonics of the 16.0 GHz carrier:		
32.0 GHz (2nd harmonic)	_____dBc	–50 dBc
Set F1 to 20.0 GHz Record the level of all harmonics of the 20.0 GHz carrier:		
40.0 GHz (2nd harmonic)	_____dBc	–50 dBc

3-10 Single Sideband Phase Noise Test

Test Procedure	Measured Value	Upper Limit
Set F1 to 0.6 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–89 dBc
1 kHz	_____dBc	–109 dBc
10 kHz	_____dBc	–109 dBc
100 kHz	_____dBc	–114 dBc
Set F1 to 2.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–83 dBc
1 kHz	_____dBc	–103 dBc
10 kHz	_____dBc	–103 dBc
100 kHz	_____dBc	–108 dBc
Set F1 to 6.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–75 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 10.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–71 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 20.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–63 dBc
1 kHz	_____dBc	–92 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc

3-10 Single Sideband Phase Noise Test (Continued)

Test Procedure	Measured Value	Upper Limit
Set F1 to 26.5 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–60 dBc
1 kHz	_____dBc	–88 dBc
10 kHz	_____dBc	–91 dBc
100 kHz	_____dBc	–93 dBc

3-11 Power Level Accuracy and Flatness Tests (Model 69085A/69185A without Option 2D Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz		Set F1 to 25.0 GHz		Set F1 to 55.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+10 dBm	_____dBm	+ 2.5 dBm	_____dBm	+ 2 dBm	_____dBm
+ 9 dBm	_____dBm	+ 1.5 dBm	_____dBm	+ 1 dBm	_____dBm
+ 8 dBm	_____dBm	+ 0.5 dBm	_____dBm	+ 0 dBm	_____dBm
+ 7 dBm	_____dBm	– 0.5 dBm	_____dBm	– 1 dBm	_____dBm
+ 6 dBm	_____dBm	– 1.5 dBm	_____dBm	– 2 dBm	_____dBm
+ 5 dBm	_____dBm	– 2.5 dBm	_____dBm	– 3 dBm	_____dBm
+ 4 dBm	_____dBm	– 3.5 dBm	_____dBm	– 4 dBm	_____dBm
+ 3 dBm	_____dBm	– 4.5 dBm	_____dBm	– 5 dBm	_____dBm
+ 2 dBm	_____dBm	– 5.5 dBm	_____dBm	– 6 dBm	_____dBm
+ 1 dBm	_____dBm	– 6.5 dBm	_____dBm	– 7 dBm	_____dBm
0 dBm	_____dBm	– 7.5 dBm	_____dBm	– 8 dBm	_____dBm
– 1 dBm	_____dBm	– 8.5 dBm	_____dBm	– 9 dBm	_____dBm
– 2 dBm	_____dBm	– 9.5 dBm	_____dBm	– 10 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.5 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+ 2 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB (0.5 to 40 GHz); 2.2 dB (40 to 60 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69185A only)

Set L1 to:	Max Power	Min Power	Variation ***
+ 2 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (0.5 to 20 GHz); 4.0 dB (20 to 40 GHz); 5.0 dB (40 to 60 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69085A/69185A with Option 2D Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz		Set F1 to 25.0 GHz		Set F1 to 55.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+ 8.5 dBm	_____dBm	+ 0 dBm	_____dBm	– 2.0 dBm	_____dBm
+ 7.5 dBm	_____dBm	– 1 dBm	_____dBm	– 3.0 dBm	_____dBm
+ 6.5 dBm	_____dBm	– 2 dBm	_____dBm	– 4.0 dBm	_____dBm
+ 5.5 dBm	_____dBm	– 3 dBm	_____dBm	– 5.0 dBm	_____dBm
+ 4.5 dBm	_____dBm	– 4 dBm	_____dBm	– 6.0 dBm	_____dBm
+ 3.5 dBm	_____dBm	– 5 dBm	_____dBm	– 7.0 dBm	_____dBm
+ 2.5 dBm	_____dBm	– 6 dBm	_____dBm	– 8.0 dBm	_____dBm
+ 1.5 dBm	_____dBm	– 7 dBm	_____dBm	– 9.0 dBm	_____dBm
+ 0.5 dBm	_____dBm	– 8 dBm	_____dBm	–10.0 dBm	_____dBm
– 0.5 dBm	_____dBm	– 9 dBm	_____dBm	–11.0 dBm	_____dBm
– 1.5 dBm	_____dBm	–10 dBm	_____dBm	–12.0 dBm	_____dBm
– 2.5 dBm	_____dBm	– 11 dBm	_____dBm	–13.0 dBm	_____dBm
– 3.5 dBm	_____dBm	– 12 dBm	_____dBm	–14.0 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.5 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
– 2 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB (0.5 to 40 GHz); 2.2 dB (40 to 60 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69185A only)

Set L1 to:	Max Power	Min Power	Variation ***
– 2 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 6.0 dB (0.5 to 20 GHz); 8.2 dB (20 to 40 GHz); 10.2 dB (40 to 60 GHz)(typical, not a specification).

ANRITSU Model 69085A/69185A **Date:** _____

Serial Number _____ **Calibrated By:** _____

4-7 Preliminary Calibration

Procedure Step	**Step Completion**
1. Internal DVM Calibration (calterm119)	_____
2. Fine Loop Pretune DAC Calibration (calterm 136)	_____
3. Sweep Time DAC Calibration (calterm 132)	_____
4. YIG Frequency Offset DAC Calibration (calterm 134)	_____
5. YIG Frequency Linearizer DACs Calibration (calterm 127)	_____
6. 100 MHz Reference Oscillator Calibration (calterm 130)	_____
7. Ramp Center DAC Calibration (calterm 129)	_____
8. Sweep Width DAC Calibration (calterm 133)	_____
9. Center Frequency DAC Calibration (calterm 114)	_____
10. Store the Calibration Data	_____

4-8 Switched Filter Shaper Calibration

Log Amplifier Zero Calibration **Step Completion**

1. Log Amplifier Zero Calibration (calterm 115) . . . . . _____

Limiter DAC Adjustment

2. Limiter DAC Adjustment (calterm 145). . . . . _____

Shaper DAC Adjustment

2. Shaper DAC Adjustment (calterm 138) . . . . . .
3. Store the Calibration Data . . . . . _____

4-9 RF Level Calibration

This calibration is performed using an automatic test system. Contact ANRITSU Customer Service for further information.

4-10 ALC Slope Calibration (69185A)

Procedure Step **Step Completion**

5. ALC Slope DAC adjustment . . . . . _____
6. Store the DAC setting value(s). . . . . _____

4-11 ALC Bandwidth Calibration

Procedure Step **Step Completion**

1. ALC Bandwidth Calibration (Calterm 110) . . . . . _____
2. Store the Calibration Data . . . . . _____

4-12 AM Calibration (69185A)

Procedure Step	Step Completion
2. Linear AM Calibration (calterm 112)	_____
3. Log AM Calibration (calterm 113)	_____
4. AM Meter Calibration (calterm 147)	_____
5. Store the Calibration Data	_____

4-13 FM Calibration (69185A)

Procedure Step	Step Completion
1. FM Meter Calibration (calterm 123)	_____
2. FM Variable Gain Linearity Calibration (calterm 148)	_____
3. FM Wide Sensitivity Calibration (calterm 124)	_____
4. FM Narrow Sensitivity Calibration (calterm 125)	_____
5. FM Rear Panel Input Gain Calibration (calterm 149)	_____
6. Store the Calibration Data	_____

ANRITSU Model 69087A/69187A **Date:** _____

Serial Number _____ **Tested By:** _____

3-6 Internal Time Base Aging Rate Test

Test Procedure	Measured Value	Upper Limit
Record frequency error value	_____	
Record frequency error value (after 24 hours)	_____	
Record the computed aging rate	_____per day	$2x10^{-8}$ per day ($5x10^{-10}$ per day with Option 16)

3-7 Frequency Synthesis Tests

Coarse Loop/YIG Loop Test Procedure

Test Frequency (in GHz)	Measured Value *	Test Frequency (in GHz)	Measured Value *
1.000 000 000	_____	26.000 000 000	_____
2.000 000 000	_____	27.000 000 000	_____
3.000 000 000	_____	28.000 000 000	_____
4.000 000 000	_____	29.000 000 000	_____
5.000 000 000	_____	30.000 000 000	_____
6.000 000 000	_____	31.000 000 000	_____
7.000 000 000	_____	32.000 000 000	_____
8.000 000 000	_____	33.000 000 000	_____
9.000 000 000	_____	34.000 000 000	_____
10.000 000 000	_____	35.000 000 000	_____
11.000 000 000	_____	36.000 000 000	_____
12.000 000 000	_____	37.000 000 000	_____
13.000 000 000	_____	38.000 000 000	_____
14.000 000 000	_____	39.000 000 000	_____
15.000 000 000	_____	40.000 000 000	_____
16.000 000 000	_____	41.000 000 000	_____
17.000 000 000	_____	42.000 000 000	_____
18.000 000 000	_____	43.000 000 000	_____
19.000 000 000	_____	44.000 000 000	_____
20.000 000 000	_____	45.000 000 000	_____
21.000 000 000	_____	46.000 000 000	_____
22.000 000 000	_____	47.000 000 000	_____
23.000 000 000	_____	48.000 000 000	_____
24.000 000 000	_____	49.000 000 000	_____
25.000 000 000	_____	50.000 000 000	_____

3-7 Frequency Synthesis Tests (Continued)

Coarse Loop/YIG Loop Test Procedure (Continued)

Test Frequency (in GHz)	Measured Value *	Test Frequency (in GHz)	Measured Value *
51.000 000 000	_____	56.000 000 000	_____
52.000 000 000	_____	57.000 000 000	_____
53.000 000 000	_____	58.000 000 000	_____
54.000 000 000	_____	59.000 000 000	_____
55.000 000 000	_____	60.000 000 000	_____

* Specification for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (Standard 69X87A)

Test Frequency (in Ghz)	Measured Value **
1.000 001 000	_____
1.000 002 000	_____
1.000 003 000	_____
1.000 004 000	_____
1.000 005 000	_____
1.000 006 000	_____
1.000 007 000	_____
1.000 008 000	_____
1.000 009 000	_____
1.000 010 000	_____
	_____

** Specifications for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (69X87A with Option 11)

Test Frequency (in Ghz)	Measured Value ***
1.000 000 100	_____
1.000 000 200	_____
1.000 000 300	_____
1.000 000 400	_____
1.000 000 500	_____
1.000 000 600	_____
1.000 000 700	_____
1.000 000 800	_____
1.000 000 900	_____
1.000 001 000	_____

*** Specification for all frequencies listed above is ±10 Hz.

3-8 Spurious Signals Test: RF Output Signals <2 GHz

Test Procedure	Measured Value	Upper Limit
Set F1 to 10 MHz Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 20 MHz Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 30 MHz Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 40 MHz Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 350 MHz Record the presence of the worst case harmonic	_____dBc	–40 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 1.6 GHz Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 1.6 GHz Record the level of the harmonics of the 1.6 GHz carrier: 3.2 GHz (2nd harmonic)	_____dBc	–40 dBc
4.8 GHz (3rd harmonic)	_____dBc	–40 dBc

3-9 Harmonic Test: RF Output Signals From 2 to 20 GHz

Test Procedure (2 to 10 GHz)	**Measure Value**	**Upper Limit**
Set F1 to 2.1 GHz Record the level of all harmonics of the 2.1 GHz carrier:		
4.2 GHz (2nd harmonic)	_____dBc	–50 dBc
6.3 GHz (3rd harmonic)	_____dBc	–50 dBc
8.4 GHz (4th harmonic)	_____dBc	–50 dBc
10.5 GHz (5th harmonic)	_____dBc	–50 dBc
12.6 GHz (6th harmonic)	_____dBc	–50 dBc
14.7 GHz (7th harmonic)	_____dBc	–50 dBc
16.8 GHz (8th harmonic)	_____dBc	–50 dBc
18.9 GHz (9th harmonic)	_____dBc	–50 dBc
Set F1 to 3.6 GHz Record the level of all harmonics of the 3.6 GHz carrier:		
7.2 GHz (2nd harmonic)	_____dBc	–50 dBc
10.8 GHz (3rd harmonic)	_____dBc	–50 dBc
14.4 GHz (4th harmonic)	_____dBc	–50 dBc
18.0 Ghz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 7.0 GHz Record the level of all harmonics of the 7 GHz carrier:		
14.0 GHz (2nd harmonic)	_____dBc	–50 dBc
Set F1 to 10.0 GHz Record the level of all harmonics of the 10 GHz carrier:		
20.0 GHz (2nd harmonic)	_____dBc	–50 dBc

Test Procedure (11 to 20 GHz)		
Set F1 to 12.4 GHz Record the level of all harmonics of the 12.4 GHz carrier:		
24.8 GHz (2nd harmonic)	_____dBc	–50 dBc
37.2 GHz (3rd harmonic)	_____dBc	–50 dBc
Set F1 to 16.0 GHz Record the level of all harmonics of the 16.0 GHz carrier:		
32.0 GHz (2nd harmonic)	_____dBc	–50 dBc
Set F1 to 20.0 GHz Record the level of all harmonics of the 20.0 GHz carrier:		
40.0 GHz (2nd harmonic)	_____dBc	–50 dBc

3-10 Single Sideband Phase Noise Test

Test Procedure	Measured Value	Upper Limit
Set F1 to 0.6 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–77 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc
Set F1 to 2.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–77 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 6.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–75 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 10.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–71 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 20.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–63 dBc
1 kHz	_____dBc	–92 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc

3-10 Single Sideband Phase Noise Test (Continued)

Test Procedure	Measured Value	Upper Limit
Set F1 to 26.5 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–60 dBc
1 kHz	_____dBc	–88 dBc
10 kHz	_____dBc	–91 dBc
100 kHz	_____dBc	–93 dBc

3-11 Power Level Accuracy and Flatness Tests (Model 69087A/69187A without Option 2D Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz		Set F1 to 25.0 GHz		Set F1 to 55.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+10 dBm	_____dBm	+ 2.5 dBm	_____dBm	+ 2 dBm	_____dBm
+ 9 dBm	_____dBm	+ 1.5 dBm	_____dBm	+ 1 dBm	_____dBm
+ 8 dBm	_____dBm	+ 0.5 dBm	_____dBm	+ 0 dBm	_____dBm
+ 7 dBm	_____dBm	– 0.5 dBm	_____dBm	– 1 dBm	_____dBm
+ 6 dBm	_____dBm	– 1.5 dBm	_____dBm	– 2 dBm	_____dBm
+ 5 dBm	_____dBm	– 2.5 dBm	_____dBm	– 3 dBm	_____dBm
+ 4 dBm	_____dBm	– 3.5 dBm	_____dBm	– 4 dBm	_____dBm
+ 3 dBm	_____dBm	– 4.5 dBm	_____dBm	– 5 dBm	_____dBm
+ 2 dBm	_____dBm	– 5.5 dBm	_____dBm	– 6 dBm	_____dBm
+ 1 dBm	_____dBm	– 6.5 dBm	_____dBm	– 7 dBm	_____dBm
0 dBm	_____dBm	– 7.5 dBm	_____dBm	– 8 dBm	_____dBm
– 1 dBm	_____dBm	– 8.5 dBm	_____dBm	– 9 dBm	_____dBm
– 2 dBm	_____dBm	– 9.5 dBm	_____dBm	– 10 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.5 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+ 2 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 1.6 dB (0.05 to 40 GHz); 2.2 dB (40 to 60 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69187A only)

Set L1 to:	Max Power	Min Power	Variation ***
+ 2 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 2.0 dB (0.05 to 20 GHz); 4.0 dB (20 to 40 GHz); 5.0 dB (40 to 60 GHz)(typical, not a specification).

3-11 Power Level Accuracy and Flatness Tests (Continued) (Model 69087A/69187A with Option 2D Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz		Set F1 to 25.0 GHz		Set F1 to 55.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+ 8.5 dBm	_____dBm	+ 0 dBm	_____dBm	– 2.0 dBm	_____dBm
+ 7.5 dBm	_____dBm	– 1 dBm	_____dBm	– 3.0 dBm	_____dBm
+ 6.5 dBm	_____dBm	– 2 dBm	_____dBm	– 4.0 dBm	_____dBm
+ 5.5 dBm	_____dBm	– 3 dBm	_____dBm	– 5.0 dBm	_____dBm
+ 4.5 dBm	_____dBm	– 4 dBm	_____dBm	– 6.0 dBm	_____dBm
+ 3.5 dBm	_____dBm	– 5 dBm	_____dBm	– 7.0 dBm	_____dBm
+ 2.5 dBm	_____dBm	– 6 dBm	_____dBm	– 8.0 dBm	_____dBm
+ 1.5 dBm	_____dBm	– 7 dBm	_____dBm	– 9.0 dBm	_____dBm
+ 0.5 dBm	_____dBm	– 8 dBm	_____dBm	–10.0 dBm	_____dBm
– 0.5 dBm	_____dBm	– 9 dBm	_____dBm	–11.0 dBm	_____dBm
– 1.5 dBm	_____dBm	–10 dBm	_____dBm	–12.0 dBm	_____dBm
– 2.5 dBm	_____dBm	– 11 dBm	_____dBm	–13.0 dBm	_____dBm
– 3.5 dBm	_____dBm	– 12 dBm	_____dBm	–14.0 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.5 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
– 2 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 1.6 dB (0.05 to 40 GHz); 2.2 dB (40 to 60 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69187A only)

Set L1 to:	Max Power	Min Power	Variation ***
– 2 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 7.0 dB (0.01 to 0.05 GHz); 6.0 dB (0.05 to 20 GHz); 8.2 dB (20 to 40 GHz); 10.2 dB (40 to 60 GHz)(typical, not a specification).

ANRITSU Model 69087A/69187A **Date:** _____

Serial Number _____ **Calibrated By:** _____

4-7 Preliminary Calibration

Procedure Step	**Step Completion**
1. Internal DVM Calibration (calterm119)	_____
2. Fine Loop Pretune DAC Calibration (calterm 136)	_____
3. Sweep Time DAC Calibration (calterm 132)	_____
4. YIG Frequency Offset DAC Calibration (calterm 134)	_____
5. YIG Frequency Linearizer DACs Calibration (calterm 127)	_____
6. 100 MHz Reference Oscillator Calibration (calterm 130)	_____
7. Ramp Center DAC Calibration (calterm 129)	_____
8. Sweep Width DAC Calibration (calterm 133)	_____
9. Center Frequency DAC Calibration (calterm 114)	_____
10. Store the Calibration Data	_____

4-8 Switched Filter Shaper Calibration

Log Amplifier Zero Calibration **Step Completion**

1. Log Amplifier Zero Calibration (calterm 115) . . . . . _____

Limiter DAC Adjustment

2. Limiter DAC Adjustment (calterm 145). . . . . _____

Shaper DAC Adjustment

2. Shaper DAC Adjustment (calterm 138) . . . . . _____
3. Store the Calibration Data . . . . . _____

4-9 RF Level Calibration

This calibration is performed using an automatic test system. Contact ANRITSU Customer Service for further information.

4-10 ALC Slope Calibration (69187A)

Procedure Step **Step Completion**

5. ALC Slope DAC adjustment . . . . . _____
6. Store the DAC setting value(s). . . . . _____

4-11 ALC Bandwidth Calibration

Procedure Step **Step Completion**

1. ALC Bandwidth Calibration (Calterm 110) . . . . . _____
2. Store the Calibration Data . . . . . _____

4-12 AM Calibration (69187A)

Procedure Step	Step Completion
2. Linear AM Calibration (calterm 112)	_____
3. Log AM Calibration (calterm 113)	_____
4. AM Meter Calibration (calterm 147)	_____
5. Store the Calibration Data	_____

4-13 FM Calibration (69187A)

Procedure Step	Step Completion
1. FM Meter Calibration (calterm 123)	_____
2. FM Variable Gain Linearity Calibration (calterm 148)	_____
3. FM Wide Sensitivity Calibration (calterm 124)	_____
4. FM Narrow Sensitivity Calibration (calterm 125)	_____
5. FM Rear Panel Input Gain Calibratioin (calterm 149)	_____
6. Store the Calibration Data	_____

ANRITSU Model 69095A/69195A **Date:** _____

Serial Number _____ **Tested By:** _____

3-6 Internal Time Base Aging Rate Test

Test Procedure	Measured Value	Upper Limit
Record frequency error value	_____	
Record frequency error value (after 24 hours)	_____	
Record the computed aging rate	_____per day	$2x10^{-8}$ per day ($5x10^{-10}$ per day with Option 16)

3-7 Frequency Synthesis Tests

Coarse Loop/YIG Loop Test Procedure

Test Frequency (in GHz)	Measured Value *	Test Frequency (in GHz)	Measured Value *
1.000 000 000	_____	26.000 000 000	_____
2.000 000 000	_____	27.000 000 000	_____
3.000 000 000	_____	28.000 000 000	_____
4.000 000 000	_____	29.000 000 000	_____
5.000 000 000	_____	30.000 000 000	_____
6.000 000 000	_____	31.000 000 000	_____
7.000 000 000	_____	32.000 000 000	_____
8.000 000 000	_____	33.000 000 000	_____
9.000 000 000	_____	34.000 000 000	_____
10.000 000 000	_____	35.000 000 000	_____
11.000 000 000	_____	36.000 000 000	_____
12.000 000 000	_____	37.000 000 000	_____
13.000 000 000	_____	38.000 000 000	_____
14.000 000 000	_____	39.000 000 000	_____
15.000 000 000	_____	40.000 000 000	_____
16.000 000 000	_____	41.000 000 000	_____
17.000 000 000	_____	42.000 000 000	_____
18.000 000 000	_____	43.000 000 000	_____
19.000 000 000	_____	44.000 000 000	_____
20.000 000 000	_____	45.000 000 000	_____
21.000 000 000	_____	46.000 000 000	_____
22.000 000 000	_____	47.000 000 000	_____
23.000 000 000	_____	48.000 000 000	_____
24.000 000 000	_____	49.000 000 000	_____
25.000 000 000	_____	50.000 000 000	_____

3-7 Frequency Synthesis Tests (Continued)

Coarse Loop/YIG Loop Test Procedure (Continued)

Test Frequency (in GHz)	Measured Value *	Test Frequency (in GHz)	Measured Value *
51.000 000 000	_____	59.000 000 000	_____
52.000 000 000	_____	60.000 000 000	_____
53.000 000 000	_____	61.000 000 000	_____
54.000 000 000	_____	62.000 000 000	_____
55.000 000 000	_____	63.000 000 000	_____
56.000 000 000	_____	64.000 000 000	_____
57.000 000 000	_____	65.000 000 000	_____
58.000 000 000	_____		

* Specification for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (Standard 69X95A)

Test Frequency (in Ghz)	Measured Value **
1.000 001 000	_____
1.000 002 000	_____
1.000 003 000	_____
1.000 004 000	_____
1.000 005 000	_____
1.000 006 000	_____
1.000 007 000	_____
1.000 008 000	_____
1.000 009 000	_____
1.000 010 000	_____
	_____

** Specifications for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (69X95A with Option 11)

Test Frequency (in Ghz)	Measured Value ***
1.000 000 100	_____
1.000 000 200	_____
1.000 000 300	_____
1.000 000 400	_____
1.000 000 500	_____
1.000 000 600	_____
1.000 000 700	_____
1.000 000 800	_____
1.000 000 900	_____
1.000 001 000	_____

*** Specification for all frequencies listed above is ±10 Hz.

3-8 Spurious Signals Test: RF Output Signals <2.2 GHz

Test Procedure	Measured Value	Upper Limit
Set F1 to 500 MHz Record the level of all harmonics of the 500 MHz carrier		
1.0 GHz (2nd harmonic)	_____dBc	–50 dBc
1.5 GHz (3rd harmonic)	_____dBc	–50 dBc
2.0 GHz (4th harmonic)	_____dBc	–50 dBc
2.5 GHz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 800 MHz Record the level of all harmonics of the 800 MHz carrier		
1.6 GHz (2nd harmonic)	_____dBc	–50 dBc
2.4 GHz (3rd harmonic)	_____dBc	–50 dBc
3.2 GHz (4th harmonic)	_____dBc	–50 dBc
4.0 GHz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 1.3 GHz Record the level of all harmonics of the 1.3 GHz carrier		
2.6 GHz (2nd harmonic)	_____dBc	–50 dBc
3.9 GHz (3rd harmonic)	_____dBc	–50 dBc
5.2 GHz (4th harmonic)	_____dBc	–50 dBc
6.5 GHz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 2.1 GHz Record the level of all harmonics of the 2.1 GHz carrier		
4.2 GHz (2nd harmonic)	_____dBc	–50 dBc
6.3 GHz (3rd harmonic)	_____dBc	–50 dBc
8.2 GHz (4th harmonic)	_____dBc	–50 dBc
10.2 GHz (5th harmonic)	_____dBc	–50 dBc

3-9 Harmonic Test: RF Output Signals From 2.2 to 20 GHz

Test Procedure (2.2 to 10 GHz)	**Measure Value**	**Upper Limit**
Set F1 to 2.4 GHz Record the level of all harmonics of the 2.4 GHz carrier:		
4.8 GHz (2nd harmonic)	_____dBc	–50 dBc
7.2 GHz (3rd harmonic)	_____dBc	–50 dBc
9.6 GHz (4th harmonic)	_____dBc	–50 dBc
12.0 GHz (5th harmonic)	_____dBc	–50 dBc
14.4 GHz (6th harmonic)	_____dBc	–50 dBc
16.8 GHz (7th harmonic)	_____dBc	–50 dBc
19.2 GHz (8th harmonic)	_____dBc	–50 dBc
Set F1 to 3.6 GHz Record the level of all harmonics of the 3.6 GHz carrier:		
7.2 GHz (2nd harmonic)	_____dBc	–50 dBc
10.8 GHz (3rd harmonic)	_____dBc	–50 dBc
14.4 GHz (4th harmonic)	_____dBc	–50 dBc
18.0 Ghz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 7.0 GHz Record the level of all harmonics of the 7 GHz carrier:		
14.0 GHz (2nd harmonic)	_____dBc	–50 dBc
Set F1 to 10.0 GHz Record the level of all harmonics of the 10 GHz carrier:		
20.0 GHz (2nd harmonic)	_____dBc	–50 dBc

Test Procedure (11 to 20 GHz)		
Set F1 to 12.4 GHz Record the level of all harmonics of the 12.4 GHz carrier:		
24.8 GHz (2nd harmonic)	_____dBc	–50 dBc
37.2 GHz (3rd harmonic)	_____dBc	–50 dBc
Set F1 to 16.0 GHz Record the level of all harmonics of the 16.0 GHz carrier:		
32.0 GHz (2nd harmonic)	_____dBc	–50 dBc
Set F1 to 20.0 GHz Record the level of all harmonics of the 20.0 GHz carrier:		
40.0 GHz (2nd harmonic)	_____dBc	–50 dBc

3-10 Single Sideband Phase Noise Test

Test Procedure	Measured Value	Upper Limit
Set F1 to 0.6 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–89 dBc
1 kHz	_____dBc	–109 dBc
10 kHz	_____dBc	–109 dBc
100 kHz	_____dBc	–114 dBc
Set F1 to 2.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–83 dBc
1 kHz	_____dBc	–103 dBc
10 kHz	_____dBc	–103 dBc
100 kHz	_____dBc	–108 dBc
Set F1 to 6.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–75 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 10.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–71 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 20.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–63 dBc
1 kHz	_____dBc	–92 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc

3-10 Single Sideband Phase Noise Test (Continued)

Test Procedure	Measured Value	Upper Limit
Set F1 to 26.5 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–60 dBc
1 kHz	_____dBc	–88 dBc
10 kHz	_____dBc	–91 dBc
100 kHz	_____dBc	–93 dBc

3-11 Power Level Accuracy and Flatness Tests (Model 69095A/69195A)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz		Set F1 to 25.0 GHz		Set F1 to 60.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+10 dBm	_____dBm	+ 2.5 dBm	_____dBm	– 2 dBm	_____dBm
+ 9 dBm	_____dBm	+ 1.5 dBm	_____dBm	– 3 dBm	_____dBm
+ 8 dBm	_____dBm	+ 0.5 dBm	_____dBm	– 4 dBm	_____dBm
+ 7 dBm	_____dBm	– 0.5 dBm	_____dBm	– 5 dBm	_____dBm
+ 6 dBm	_____dBm	– 1.5 dBm	_____dBm	– 6 dBm	_____dBm
+ 5 dBm	_____dBm	– 2.5 dBm	_____dBm	– 7 dBm	_____dBm
+ 4 dBm	_____dBm	– 3.5 dBm	_____dBm	– 8 dBm	_____dBm
+ 3 dBm	_____dBm	– 4.5 dBm	_____dBm	– 9 dBm	_____dBm
+ 2 dBm	_____dBm	– 5.5 dBm	_____dBm	– 10 dBm	_____dBm
+ 1 dBm	_____dBm	– 6.5 dBm	_____dBm	– 11 dBm	_____dBm
0 dBm	_____dBm	– 7.5 dBm	_____dBm	– 12 dBm	_____dBm
– 1 dBm	_____dBm	– 8.5 dBm	_____dBm	– 13 dBm	_____dBm
– 2 dBm	_____dBm	– 9.5 dBm	_____dBm	– 14 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.5 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
– 2 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB (0.5 to 40 GHz); 2.2 dB (40 to 65 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69195A only)

Set L1 to:	Max Power	Min Power	Variation ***
– 2 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (0.5 to 20 GHz); 4.0 dB (20 to 40 GHz); 5.0 dB (40 to 65 GHz)(typical, not a specification).

ANRITSU Model 69095A/69195A **Date:** _____

Serial Number _____ **Calibrated By:** _____

4-7 Preliminary Calibration

Procedure Step	**Step Completion**
1. Internal DVM Calibration (calterm119)	_____
2. Fine Loop Pretune DAC Calibration (calterm 136)	_____
3. Sweep Time DAC Calibration (calterm 132)	_____
4. YIG Frequency Offset DAC Calibration (calterm 134)	_____
5. YIG Frequency Linearizer DACs Calibration (calterm 127)	_____
6. 100 MHz Reference Oscillator Calibration (calterm 130)	_____
7. Ramp Center DAC Calibration (calterm 129)	_____
8. Sweep Width DAC Calibration (calterm 133)	_____
9. Center Frequency DAC Calibration (calterm 114)	_____
10. Store the Calibration Data	_____

4-8 Switched Filter Shaper Calibration

Log Amplifier Zero Calibration **Step Completion**

1. Log Amplifier Zero Calibration (calterm 115) . . . . . _____

Limiter DAC Adjustment

2. Limiter DAC Adjustment (calterm 145). . . . . _____

Shaper DAC Adjustment

2. Shaper DAC Adjustment (calterm 138) . . . . . _____
3. Store the Calibration Data . . . . . _____

4-9 RF Level Calibration

This calibration is performed using an automatic test system. Contact ANRITSU Customer Service for further information.

4-10 ALC Slope Calibration (69195A)

Procedure Step **Step Completion**

5. ALC Slope DAC adjustment . . . . . _____
6. Store the DAC setting value(s). . . . . _____

4-11 ALC Bandwidth Calibration

Procedure Step **Step Completion**

1. ALC Bandwidth Calibration (Calterm 110) . . . . . _____
2. Store the Calibration Data . . . . . _____

4-12 AM Calibration (69195A)

Procedure Step	Step Completion
2. Linear AM Calibration (calterm 112)	_____
3. Log AM Calibration (calterm 113)	_____
4. AM Meter Calibration (calterm 147)	_____
5. Store the Calibration Data	_____

4-13 FM Calibration (69195A)

Procedure Step	Step Completion
1. FM Meter Calibration (calterm 123)	_____
2. FM Variable Gain Linearity Calibration (calterm 148)	_____
3. FM Wide Sensitivity Calibration (calterm 124)	_____
4. FM Narrow Sensitivity Calibration (calterm 125)	_____
5. FM Rear Panel Input Gain Calibration (calterm 149)	_____
6. Store the Calibration Data	_____

ANRITSU Model 69097A/69197A **Date:** _____

Serial Number _____ **Tested By:** _____

3-6 Internal Time Base Aging Rate Test

Test Procedure	Measured Value	Upper Limit
Record frequency error value	_____	
Record frequency error value (after 24 hours)	_____	
Record the computed aging rate	_____per day	$2x10^{-8}$ per day ($5x10^{-10}$ per day with Option 16)

3-7 Frequency Synthesis Tests

Coarse Loop/YIG Loop Test Procedure

Test Frequency (in GHz)	Measured Value *	Test Frequency (in GHz)	Measured Value *
1.000 000 000	_____	26.000 000 000	_____
2.000 000 000	_____	27.000 000 000	_____
3.000 000 000	_____	28.000 000 000	_____
4.000 000 000	_____	29.000 000 000	_____
5.000 000 000	_____	30.000 000 000	_____
6.000 000 000	_____	31.000 000 000	_____
7.000 000 000	_____	32.000 000 000	_____
8.000 000 000	_____	33.000 000 000	_____
9.000 000 000	_____	34.000 000 000	_____
10.000 000 000	_____	35.000 000 000	_____
11.000 000 000	_____	36.000 000 000	_____
12.000 000 000	_____	37.000 000 000	_____
13.000 000 000	_____	38.000 000 000	_____
14.000 000 000	_____	39.000 000 000	_____
15.000 000 000	_____	40.000 000 000	_____
16.000 000 000	_____	41.000 000 000	_____
17.000 000 000	_____	42.000 000 000	_____
18.000 000 000	_____	43.000 000 000	_____
19.000 000 000	_____	44.000 000 000	_____
20.000 000 000	_____	45.000 000 000	_____
21.000 000 000	_____	46.000 000 000	_____
22.000 000 000	_____	47.000 000 000	_____
23.000 000 000	_____	48.000 000 000	_____
24.000 000 000	_____	49.000 000 000	_____
25.000 000 000	_____	50.000 000 000	_____

3-7 Frequency Synthesis Tests (Continued)

Coarse Loop/YIG Loop Test Procedure (Continued)

Test Frequency (in GHz)	Measured Value *	Test Frequency (in GHz)	Measured Value *
51.000 000 000	_____	59.000 000 000	_____
52.000 000 000	_____	60.000 000 000	_____
53.000 000 000	_____	61.000 000 000	_____
54.000 000 000	_____	62.000 000 000	_____
55.000 000 000	_____	63.000 000 000	_____
56.000 000 000	_____	64.000 000 000	_____
57.000 000 000	_____	65.000 000 000	_____
58.000 000 000	_____		

* Specification for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (Standard 69X97A)

Test Frequency (in Ghz)	Measured Value **
1.000 001 000	_____
1.000 002 000	_____
1.000 003 000	_____
1.000 004 000	_____
1.000 005 000	_____
1.000 006 000	_____
1.000 007 000	_____
1.000 008 000	_____
1.000 009 000	_____
1.000 010 000	_____
	_____

** Specifications for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (69X97A with Option 11)

Test Frequency (in Ghz)	Measured Value ***
1.000 000 100	_____
1.000 000 200	_____
1.000 000 300	_____
1.000 000 400	_____
1.000 000 500	_____
1.000 000 600	_____
1.000 000 700	_____
1.000 000 800	_____
1.000 000 900	_____
1.000 001 000	_____

*** Specification for all frequencies listed above is ±10 Hz.

3-8 Spurious Signals Test: RF Output Signals <2 GHz

Test Procedure	Measured Value	Upper Limit
Set F1 to 10 MHz Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 20 MHz Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 30 MHz Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 40 MHz Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 350 MHz Record the presence of the worst case harmonic	_____dBc	–40 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 1.6 GHz Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 1.6 GHz Record the level of the harmonics of the 1.6 GHz carrier: 3.2 GHz (2nd harmonic)	_____dBc	–40 dBc
4.8 GHz (3rd harmonic)	_____dBc	–40 dBc

3-9 Harmonic Test: RF Output Signals From 2 to 20 GHz

Test Procedure (2 to 10 GHz)	**Measure Value**	**Upper Limit**
Set F1 to 2.1 GHz Record the level of all harmonics of the 2.1 GHz carrier:		
4.2 GHz (2nd harmonic)	_____dBc	–50 dBc
6.3 GHz (3rd harmonic)	_____dBc	–50 dBc
8.4 GHz (4th harmonic)	_____dBc	–50 dBc
10.5 GHz (5th harmonic)	_____dBc	–50 dBc
12.6 GHz (6th harmonic)	_____dBc	–50 dBc
14.7 GHz (7th harmonic)	_____dBc	–50 dBc
16.8 GHz (8th harmonic)	_____dBc	–50 dBc
18.9 GHz (9th harmonic)	_____dBc	–50 dBc
Set F1 to 3.6 GHz Record the level of all harmonics of the 3.6 GHz carrier:		
7.2 GHz (2nd harmonic)	_____dBc	–50 dBc
10.8 GHz (3rd harmonic)	_____dBc	–50 dBc
14.4 GHz (4th harmonic)	_____dBc	–50 dBc
18.0 Ghz (5th harmonic)	_____dBc	–50 dBc
Set F1 to 7.0 GHz Record the level of all harmonics of the 7 GHz carrier:		
14.0 GHz (2nd harmonic)	_____dBc	–50 dBc
Set F1 to 10.0 GHz Record the level of all harmonics of the 10 GHz carrier:		
20.0 GHz (2nd harmonic)	_____dBc	–50 dBc

Test Procedure (11 to 20 GHz)		
Set F1 to 12.4 GHz Record the level of all harmonics of the 12.4 GHz carrier:		
24.8 GHz (2nd harmonic)	_____dBc	–50 dBc
37.2 GHz (3rd harmonic)	_____dBc	–50 dBc
Set F1 to 16.0 GHz Record the level of all harmonics of the 16.0 GHz carrier:		
32.0 GHz (2nd harmonic)	_____dBc	–50 dBc
Set F1 to 20.0 GHz Record the level of all harmonics of the 20.0 GHz carrier:		
40.0 GHz (2nd harmonic)	_____dBc	–50 dBc

3-10 Single Sideband Phase Noise Test

Test Procedure	Measured Value	Upper Limit
Set F1 to 0.6 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–77 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc
Set F1 to 2.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–77 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 6.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–75 dBc
1 kHz	_____dBc	–97 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 10.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–71 dBc
1 kHz	_____dBc	–95 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–102 dBc
Set F1 to 20.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–63 dBc
1 kHz	_____dBc	–92 dBc
10 kHz	_____dBc	–97 dBc
100 kHz	_____dBc	–99 dBc

3-10 Single Sideband Phase Noise Test (Continued)

Test Procedure	Measured Value	Upper Limit
Set F1 to 26.5 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–60 dBc
1 kHz	_____dBc	–88 dBc
10 kHz	_____dBc	–91 dBc
100 kHz	_____dBc	–93 dBc

3-11 Power Level Accuracy and Flatness Tests (Model 69097A/69197A)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz		Set F1 to 25.0 GHz		Set F1 to 60.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+10 dBm	_____dBm	+ 2.5 dBm	_____dBm	– 2 dBm	_____dBm
+ 9 dBm	_____dBm	+ 1.5 dBm	_____dBm	– 3 dBm	_____dBm
+ 8 dBm	_____dBm	+ 0.5 dBm	_____dBm	– 4 dBm	_____dBm
+ 7 dBm	_____dBm	– 0.5 dBm	_____dBm	– 5 dBm	_____dBm
+ 6 dBm	_____dBm	– 1.5 dBm	_____dBm	– 6 dBm	_____dBm
+ 5 dBm	_____dBm	– 2.5 dBm	_____dBm	– 7 dBm	_____dBm
+ 4 dBm	_____dBm	– 3.5 dBm	_____dBm	– 8 dBm	_____dBm
+ 3 dBm	_____dBm	– 4.5 dBm	_____dBm	– 9 dBm	_____dBm
+ 2 dBm	_____dBm	– 5.5 dBm	_____dBm	– 10 dBm	_____dBm
+ 1 dBm	_____dBm	– 6.5 dBm	_____dBm	– 11 dBm	_____dBm
0 dBm	_____dBm	– 7.5 dBm	_____dBm	– 12 dBm	_____dBm
– 1 dBm	_____dBm	– 8.5 dBm	_____dBm	– 13 dBm	_____dBm
– 2 dBm	_____dBm	– 9.5 dBm	_____dBm	– 14 dBm	_____dBm
* Specification is ±1.0 dB.		* Specification is ±1.0 dB.		* Specification is ±1.5 dB.	

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
– 2 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 1.6 dB (0.05 to 40 GHz); 2.2 dB (40 to 65 GHz).

Power Level Flatness Test Procedure (Analog Sweep) (Model 69187A only)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
– 2 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 4.0 dB (0.01 to 0.05 GHz); 2.0 dB (0.05 to 20 GHz); 4.0 dB (20 to 40 GHz); 5.0 dB (40 to 65 GHz)(typical, not a specification).

ANRITSU Model 69097A/69197A **Date:** _____

Serial Number _____ **Calibrated By:** _____

4-7 Preliminary Calibration

Procedure Step	**Step Completion**
1. Internal DVM Calibration (calterm119)	_____
2. Fine Loop Pretune DAC Calibration (calterm 136)	_____
3. Sweep Time DAC Calibration (calterm 132)	_____
4. YIG Frequency Offset DAC Calibration (calterm 134)	_____
5. YIG Frequency Linearizer DACs Calibration (calterm 127)	_____
6. 100 MHz Reference Oscillator Calibration (calterm 130)	_____
7. Ramp Center DAC Calibration (calterm 129)	_____
8. Sweep Width DAC Calibration (calterm 133)	_____
9. Center Frequency DAC Calibration (calterm 114)	_____
10. Store the Calibration Data	_____

4-8 Switched Filter Shaper Calibration

Log Amplifier Zero Calibration **Step Completion**

1. Log Amplifier Zero Calibration (calterm 115) . . . . . _____

Limiter DAC Adjustment

2. Limiter DAC Adjustment . . . . . _____

Shaper DAC Adjustment

2. Shaper DAC Adjustment (calterm 138) . . . . . _____
3. Store the Calibration Data . . . . . _____

4-9 RF Level Calibration

This calibration is performed using an automatic test system. Contact ANRITSU Customer Service for further information.

4-10 ALC Slope Calibration (69197A)

Procedure Step **Step Completion**

5. ALC Slope DAC adjustment . . . . . _____
6. Store the DAC setting value(s). . . . . _____

4-11 ALC Bandwidth Calibration

Procedure Step **Step Completion**

1. ALC Bandwidth Calibration (Calterm 110) . . . . . _____
2. Store the Calibration Data . . . . . _____

4-12 AM Calibration (69197A)

Procedure Step	Step Completion
2. Linear AM Calibration (calterm 112)	_____
3. Log AM Calibration (calterm 113)	_____
4. AM Meter Calibration (calterm 147)	_____
5. Store the Calibration Data	_____

4-13 FM Calibration (69197A)

Procedure Step	Step Completion
1. FM Meter Calibration (calterm 123)	_____
2. FM Variable Gain LInearity Calibration (calterm 148)	_____
3. FM Wide Sensitivity Calibration (calterm 124)	_____
4. FM Narrow Sensitivity Calibration (calterm 125)	_____
5. FM Rear Panel Input Gain Calibration (calterm 149)	_____
6. Store the Calibration Data	_____

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